



Design Example Report

Title	<i>60 W Isolated StackFET™ Flyback Power Supply Using InnoSwitch™3-EP Powi-GaN™ INN3679C-H606 and MinE-CAP™ MIN1072M</i>
Specification	90 VAC – 440 VAC Input; 24 V, 2.5 A Output
Application	Adapters
Author	Applications Engineering Department
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Summary and Features

- 60 W output power capability at 24 V
- Very wide input voltage range from 90 VAC up to 440 VAC
- Very high power density design enabled by MinE-CAP MIN1072M
- > 90% average efficiency at nominal AC inputs
- < 100 mW no-load input power at nominal AC inputs
- Integrated protection and reliability features
 - Output short-circuit, overvoltage protection, over-temperature shutdown
- Synchronous rectification for higher efficiency
- Input voltage monitor with accurate brown-in/brown-out protection
- Meets EN55022 and CISPR-22 Class B conducted EMI
- Meets IEC 5.0 kV Combination Wave Surge Class A
- ±15 kV ESD Class B

PATENT INFORMATION

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Important Note: Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.



1 Introduction

This engineering report describes an isolated StackFET™ configuration flyback converter designed to provide a 24 V 2.5 A output from a very wide input voltage range of 90 VAC to 440 VAC. This power supply utilizes the INN3679C-H606 from the InnoSwitch3-EP family of IC's and the MinE-CAP MIN1072M.

This document contains the complete power supply specifications, bill of materials, transformer construction, circuit schematic and printed circuit board layout, along with performance data and electrical waveforms.

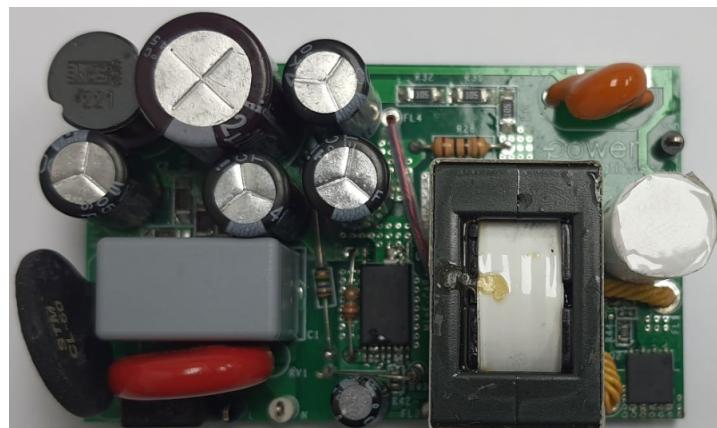


Figure 1 – Prototype Top View.

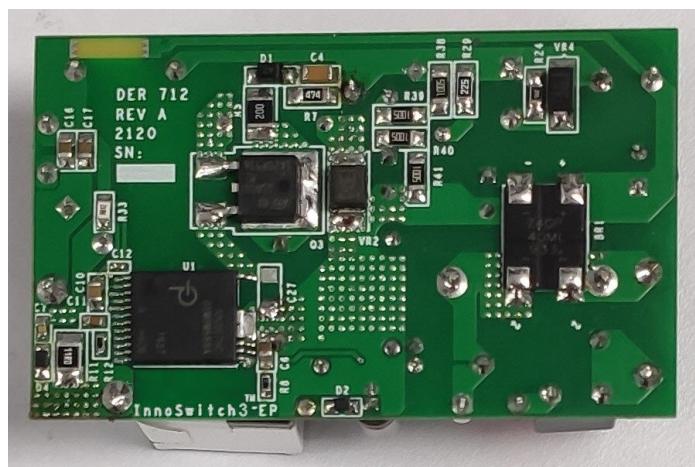


Figure 2 – Prototype Bottom View.

Note: PCB vias should be solder-filled.



2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Nom	Max	Units	Comment
Input						
Voltage	V_{IN}	90	115/230	440	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				<100	mW	
Output						
Output Voltage	V_{OUT}	22.8	24	25.2	V	$\pm 5\%$
Output Ripple Voltage	V_{RIPPLE}			600	mV	20 MHz Bandwidth.
Output Current	I_{OUT}			2.5	A	
Total Output Power						
Continuous Output Power	P_{OUT}			60	W	
Minimum Efficiency						
Full Load @ 90 VAC		89				
Full Load @ 115 VAC		90.5				
Full Load @ 230 VAC		90.5				
Full Load @ 440 VAC		89				
Average @ 115 VAC		90.5			%	Measured at P_{OUT} 25 °C.
Average @ 230 VAC		90				
Environmental						
Conducted EMI			Meets CISPR22B / EN55022B			
Surge (Differential)				5	kV	1.2/50 μ s Surge, IEC 61000-4-5, Impedance: 2 Ω Class A
ESD – Air Discharge				± 15	kV	
ESD – Contact Discharge				± 8	kV	
Ambient Temperature	T_{AMB}	0		40	°C	Free Convection, Sea Level.



3 Schematic

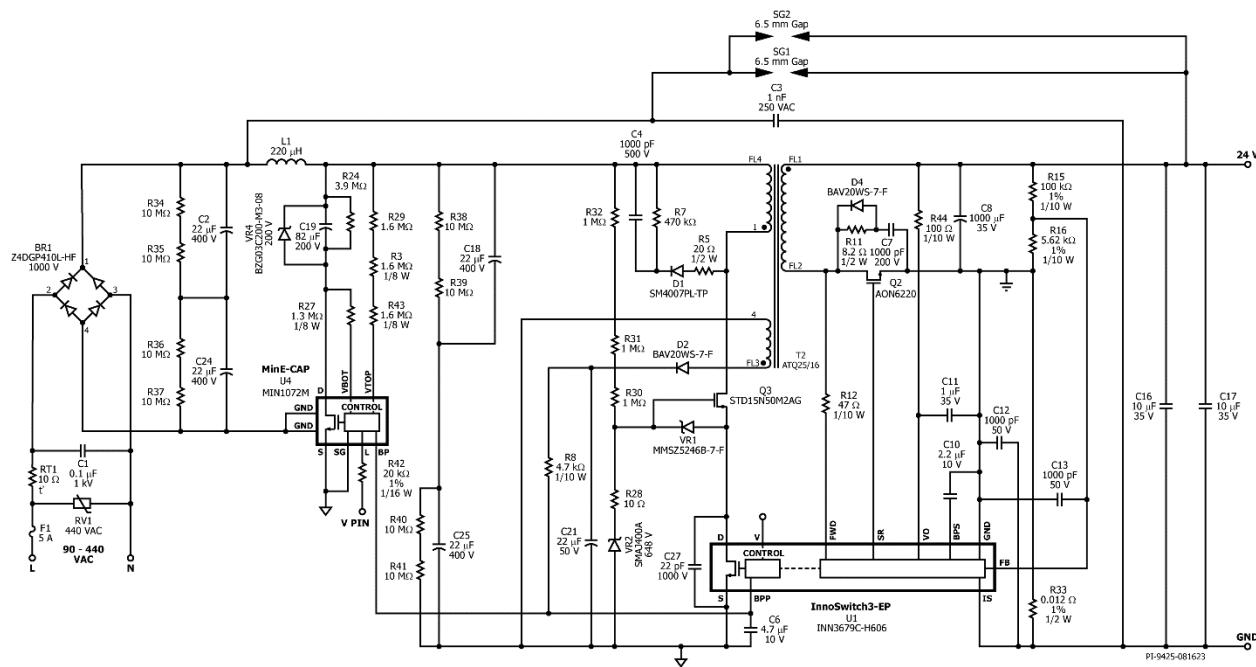


Figure 3 – Schematic.



4 Circuit Description

The InnoSwitch3-EP IC combines primary, secondary and feedback circuits in a single surface mounted off-line flyback switcher IC. The IC incorporates the primary MOSFET, the primary-side controller, the secondary-side controller for synchronous rectification, and the Fluxlink™ technology which eliminates the optocoupler needed on a secondary-sensed feedback system.

4.1 *Input Rectifier, Filter, and Surge Suppression Circuit*

Fuse F1 isolates the circuit and provides protection from component failure. Surge suppression components RV1 and RT1 protects the circuit from hazardous voltages from the AC input. Bridge rectifier BR1 converts the AC line voltage into the DC voltage seen across the input filter network. EMI filtering is provided by the X capacitor C1 and mainly by the pi filter combination of C2 and C24, L1, and C18 and C25. Capacitor C19 further bolsters EMI suppression at lower input voltages.

4.2 *MinE-CAP MIN1072M*

The MinE-CAP U4 basically connects the low voltage capacitor (LV cap) C19 when the input voltage is low and disconnects it when the input voltage is high. Connecting R42 in between the MinE-CAP L pin and InnoSwitch3-EP IC V pin disables the undervoltage and overvoltage sensing of the InnoSwitch3-EP IC. Start-up sequence however is still dictated by the MinE-CAP via its UVLO threshold levels, which still allows for the reduction of inrush currents by way of controlled charging of the LV caps. Information needed for proper control is provided by the network of sense resistors R27, R29, R3, and R43 via the voltages measured on the V_{TOP} and V_{BOT} pins. Resistor R24 is a bleeder resistor used to help regulate the voltage across the LV cap.

4.3 *InnoSwitch3-EP Primary-Side*

The primary-side of INN3679C combines a high-voltage power MOSFET and the primary-side controller into a low cost monolithic IC. The MOSFET Q3 is a cascode connected between the transformer and the INN3679C drain. This StackFET configuration increases the effective Drain-Source voltage rating of the primary switch to 1250 V_{PK}.

When AC is first applied, the INN3679C IC's internal current source connected to the DRAIN (D) is charged via the string consisting of R32, R31, R30, and the C_{ISS} of Q3. The internal regulator then charges C6 and powers the controller inside the IC. During steady state, the device controller will now be powered via a bias winding through the current limiting resistor R8 to minimize losses.

The power transformer T2 is designed for a flyback topology power supply. The start winding of the transformer is connected to the drain MOSFET Q3, while the end of the winding is connected to the rectified DC bus. The total voltage stress across the primary switch will be divided between Q3 and the internal MOSFET of the INN3679C IC. The voltage across the internal MOSFET of INN3679C IC however will be limited by the TVS



Clamp VR2. A low cost RCD clamp consisting of diode D1, capacitor C4, and resistors R5 and R7 limits to acceptable levels the effects of leakage energy generated by the transformer leakage inductance.

4.4 *InnoSwitch3-EP Secondary-Side*

The secondary-side of INN3679C IC provides output voltage sensing, output current sensing, and internal gate driver for a synchronous rectifier (SR) MOSFET. The secondary-side is powered by an internal 4.4 V regulator which draws current from either VOUT or the current-limited FWD pin via R12. Its output is connected to an external decoupling capacitor C10, also referred to as BPS capacitor.

The FWD pin also provides negative edge detection by sensing the transformer's secondary pin through resistor R12. The voltage sensed by the FWD pin is used for both the primary-secondary handshake at start-up, and for timing the turn-on instant of the SR FET Q2. This ensures quasi-resonant operation when operating at discontinuous conduction mode (DCM).

The SR FET Q2 is driven by the SR pin of U1. The RCD snubber consisting of R11, C7, and D4 limits the drain to source voltage spike across the SR FET.

The feedback network comprised of resistors R15 and R16, and capacitor C13 is connected between the output voltage and secondary ground. The sensed voltage across R16 is connected to the FB pin. The external current sense resistor R33 connected between the ISENSE and SECONDARY GROUND pins sets the maximum output current limit.

A low ESR capacitor C8 provides output filtering. Output voltage ripple is further reduced by the ceramic capacitors C16 and C17.



5 PCB Layout

PCB material: FR4, Thickness: 1 mm, Copper: 2 layers, 2 oz.
Max PSU Height: 23 mm

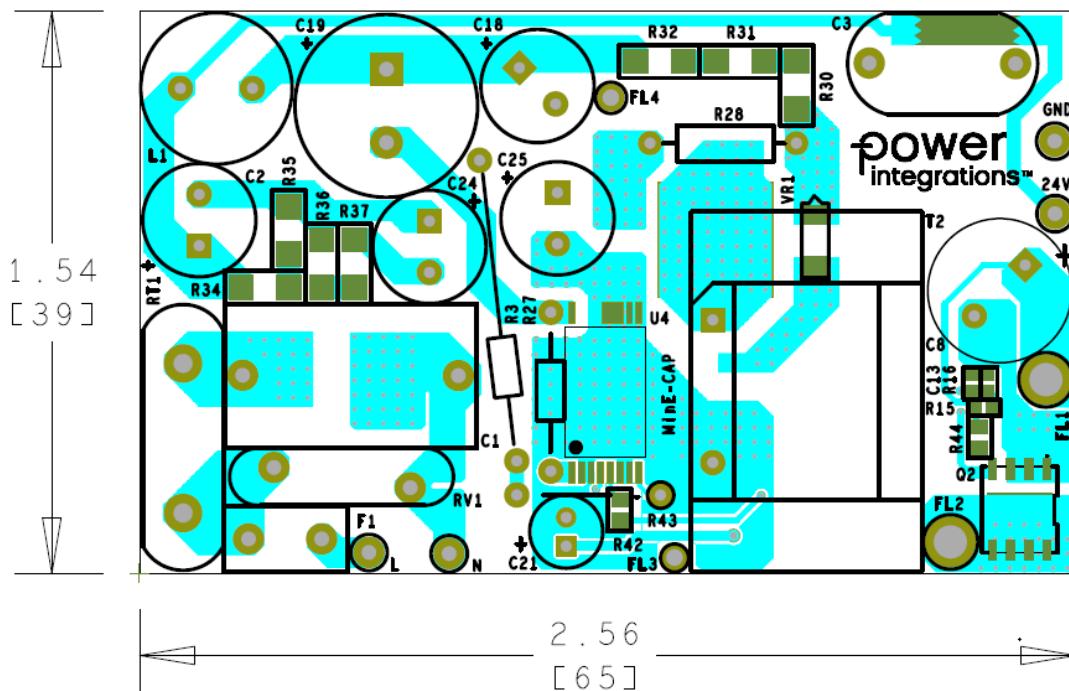


Figure 4 – Populated Circuit Board, Top View.

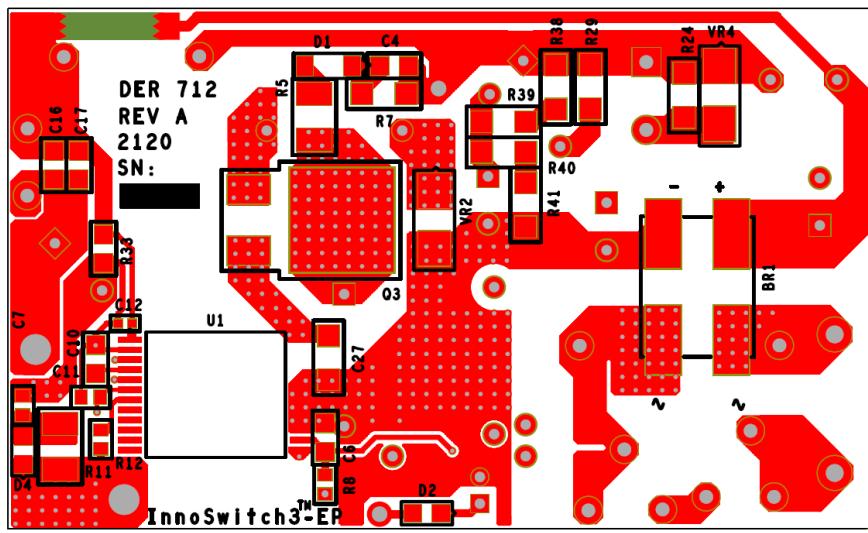


Figure 5 – Populated Circuit Board, Bottom View.



6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	RECT BRIDGE, GP, 1000 V, 4 A, Z4-D, -55°C ~ 175 °C (TJ)	Z4DGP410L-HF	Comchip
2	1	C1	0.1 µF, ±20%, 440 VAC, 1000 VDC, X1 Safety Rated, Metallized Polypropylene Film, RAD, 0.689" L x 0.394" W (17.50 mm x 10.00 mm), 0.650" (16.50 mm)	BFC233810104	Vishay
3	4	C2 C18 C24 C25	22 µF, 400 V, Electrolytic, 8 x 16	ERK2G9220F160TO	Aishi
4	1	C3	1 nF, Ceramic, Y1	440LD10-R	Vishay
5	1	C4	1000 pF, 10%, 500 V, Ceramic, X7R, 0805	C0805C102KCRACTU	Kemet
6	1	C6	4.7 µF ±10% 10 V Ceramic X7R 0805	LMK212B7475KGHT	Taiyo Yuden
7	1	C7	1000 pF, 200 V, Ceramic, X7R, 0603	06032C102KAT2A	AVX
8	1	C8	Conductive Polymer Aluminum, 1000 µF, ±20%, 35V, T/H, (10 x 16)	SPF1VM102G18000RAXXX	AiShi
9	1	C10	2.2 µF, 10 V, Ceramic, X7R, 0805	C0805C225M8RACTU	Kemet
10	1	C11	1 µF, ±10%, 35 V, Ceramic, X7R, 0603	C1608X7R1V105K080AE	TDK
11	2	C12 C13	1000 pF, ±10%, 50 V, X7R, -55°C ~ 125°C, Low ESL, 0402	C0402C102K5RACTU	Kemet
12	2	C16 C17	10 µF, 35 V, Ceramic, X5R, 0805	C2012X5R1V106K085AC	TDK
13	1	C19	82 µF, 200 V, Aluminum, Radial, Can, 12000 Hrs @ 105°C, (12.5 x 21.5, 5 mm LS), 12000 Hrs @ 105°C	UCY2D820MHD9TO	Nichicon
14	1	C21	22 µF, ±20%, 50 V, Electrolytic, Gen. Purpose, (5 x 12.5), LS 2.5 mm	UVR1H220MDD1TD	Nichicon
15	1	C27	22 pF, 1000 V, Ceramic, COG, 1206	C1206C220KDGACTU	Kemet
16	1	D1	1000 V, 1 A, Standard Recovery, SOD-123FL	SM4007PL-TP	Micro Commercial
17	2	D2 D4	200 V, 200 mW, Diode, SOD323	BAV20WS-7-F	ON Semi
18	1	F1	5 A, 250 V, Slow, Long Time Lag, RST	RST 5	Belfuse
19	1	L1	FIXED IND, 220 µH, 1.6A, 260 mΩ, TH, 7 x 10.5 mm	7447480221	Wurth
20	1	Q2	MOSFET, N-CH, 100 V, 48 A (Tc), 113.5 W (Tc), DFN5X6, 8-DFN (5x6)	AON6220	Alpha & Omega Semi
21	1	Q3	MOSFET, N-Channel 500 V, 10 A (Tc), 85 W (Tc), DPAK TO-252-3, DPak (2 Leads + Tab), SC-63	STD15N50M2AG	ST Micro
22	2	R3 R43	RES, 1.6 MΩ, 5%, 1/8 W, Carbon Film	299-1.6M-RC	Xicon
23	1	R5	RES, 20 Ω, ±5%, ½ W, 1210, Thick Film	CRCW121020R0JNEA	Vishay
24	1	R7	RES, 470 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ474V	Panasonic
25	1	R8	RES, 4.7 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ472V	Panasonic
26	1	R11	RES, 8.2 Ω, 5%, 1/2 W, Thick Film, 1210	ERJ-14YJ8R2U	Panasonic
27	1	R12	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
28	1	R15	RES, 100.0 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF1003X	Panasonic
29	1	R16	RES, 5.62 kΩ, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF5621X	Panasonic
30	1	R24	RES, 3.9 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ395V	Panasonic
31	1	R27	RES, 1.3 MΩ, 5%, 1/8 W, Carbon Film	CF18JT1M30	Stackpole
32	1	R28	RES, 10 Ω, 5%, 1/4 W, Carbon Film	CFR-25JB-10R	Yageo
33	1	R29	RES, 1.6 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ165V	Panasonic
34	3	R30 R31 R32	RES, 1.0 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ105V	Panasonic
35	1	R33	RES, 0.012 Ω, ±1%, 0.5 W, 0805, Current Sense, Metal Foil	KRL1220E-M-R012-F-T5	Susumu
36	8	R34 R35 R36 R37 R38 R39 R40 R41	RES, 10 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ106V	Panasonic
37	1	R42	RES, 20 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2002V	Panasonic



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38	1	R44	RES, 100 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ101V	Panasonic
39	1	RT1	NTC Thermistor, 10 Ω, 5 A	CL-60	GE Sensing
40	1	RV1	715 V,6 kA, Varistor, 1 Circuit, Through Hole, Disc 14 mm	V14E440P1	Littlefuse
41	1	T2	Bobbin, ATQ25/16, Horizontal, 8 pins Assembled Transformer	POL-INN051	Premier Magnetics
42	1	U1	InnoSwitch3-EP Integrated Circuit, InSOP24D	INN3679C-H606	Power Integrations
43	1	U4	MinE-CAP	MIN1072M	Power Integrations
44	1	VR1	Diode Zener 16 V 500 mW SOD123	MMSZ5246B-7-F	Diodes, Inc.
45	1	VR2	Diode, TVS,648 V Clamp, 600 mA Ipp, Surface Mount DO-214AC (SMA)	SMAJ400A	Littlefuse
46	1	VR4	Diode, Zener, 200 V, ±6%, 1.25 W, DO-214AC (SMA)	BZG03C200-M3-08	Vishay

Miscellaneous

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	24V	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone
2	2	GND L	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
3	1	N	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone



7 Transformer Specification

7.1 Electrical Diagram

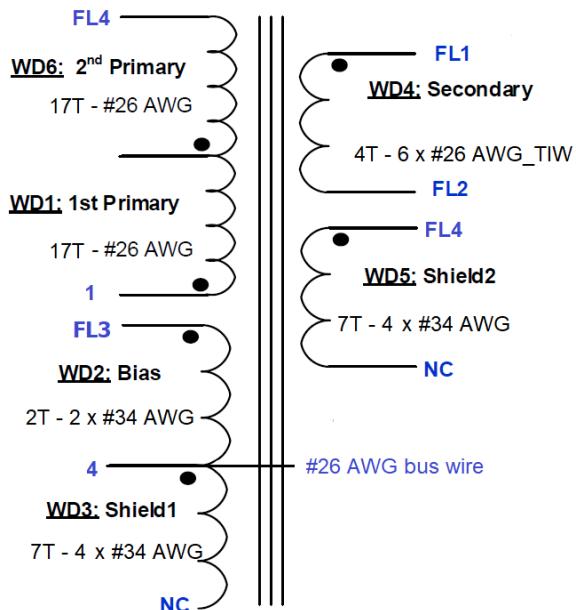


Figure 6 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V _{PK-PK} , 100 kHz switching frequency, between pin 1 and pin FL4 with all other windings open.	493 μ H
Tolerance	Tolerance of Primary Inductance.	$\pm 5\%$
Leakage Inductance	Measured across primary winding with all other windings shorted.	<6 μ H

7.3 Material List

Item	Description
[1]	Core: ATQ25/16 3C95.
[2]	Bobbin: ATQ25/16, Vertical, 8 Pins.
[3]	Magnet Wire: #26 AWG.
[4]	Magnet Wire: #34 AWG.
[5]	Tripe Insulated Wire: #26 AWG.
[6]	Polyester Tape: 8 mm.
[7]	Polyester Tape: 16.7 mm.
[8]	Polyester Tape: 10 mm x 15 mm.
[9]	Bus Wire: #26 AWG.
[10]	AWG 20 PTFE Non-Shrink Tubing: 10 mm.
[11]	AWG 24 PTFE Non-Shrink Tubing: 20 mm.
[12]	Varnish: Dolph BC 359 or Equivalent.



7.4 Transformer Build Diagram

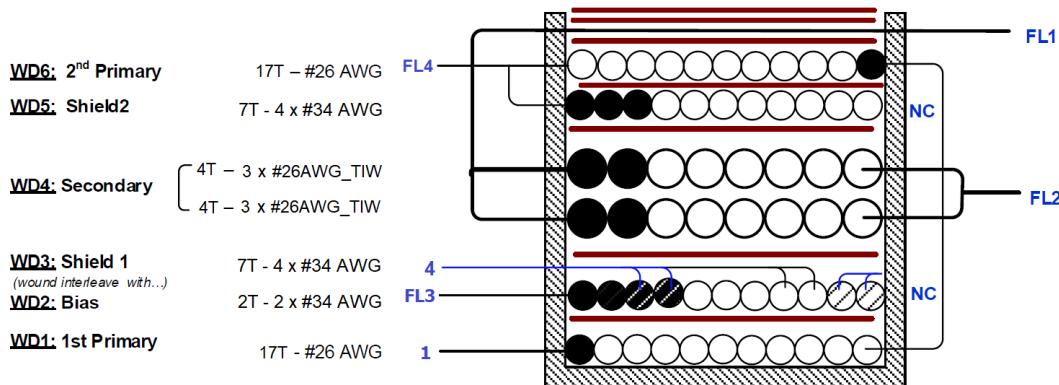


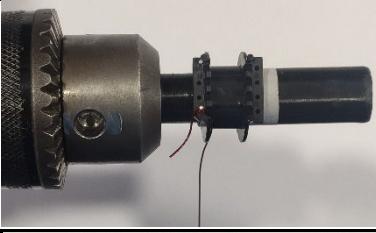
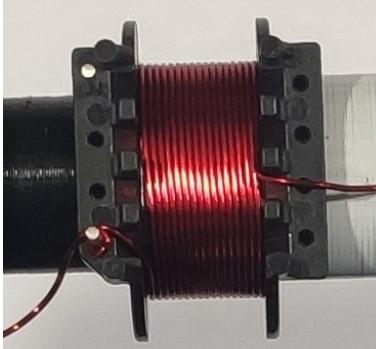
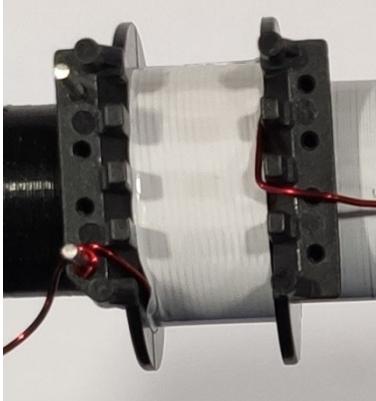
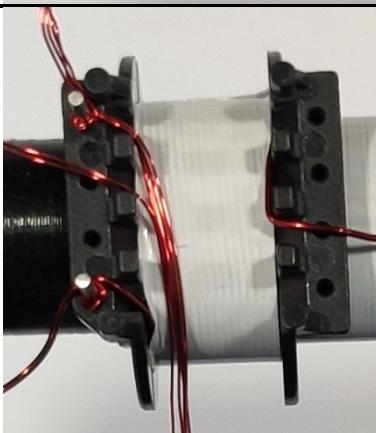
Figure 7 – Transformer Build Diagram.

7.5 Transformer Instructions

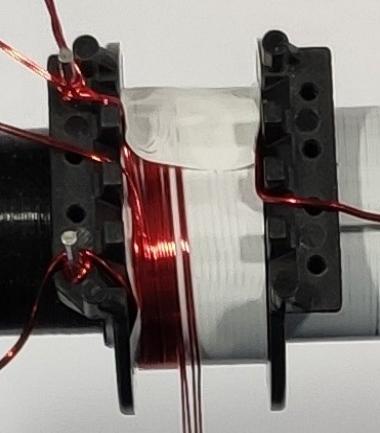
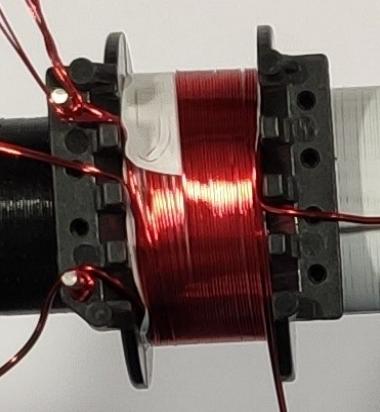
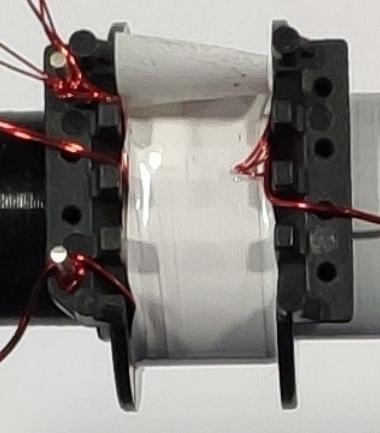
Bobbin Preparation	For the purposes of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise. Before winding, remove pins 2, 3, 5, 6, 7, and 8.
WD1 1st Primary	Start at pin 1, wind 17 turns of wire Item [3] in a single layer. Leave ~3 feet long for 2 nd primary winding.
Insulation	1 layer of tape Item [6]
WD2: Bias Winding, WD3: Shield Winding	Prepare 6 strands of wire Item [4] for both windings. For WD2, start 2 strands of the wire as FL3 and leave ~15 mm length of excess wire. For WD3, start the other 4 strands at pin 4. Wind all 6 wires in parallel. At the 2 nd turn, place a piece of tape to hold the wires and terminate WD2 to pin 4. Continue WD3 for 5 more turns and then cut the wire to leave it as No-Connect.
Insulation	1 layer of tape Item [6]
WD4 Secondary	Start at left side of the bobbin. Use 3 wires Item [5], and leave ~25 mm length of excess wire, then mark as FL1. Wind 4 trifilar turns in 1 layer, from left to right, at the last turn exit the wires at right side of the bobbin, also leaving ~15 mm and mark FL2. Repeat the same winding above on top previous winding, also mark start and finish ends as FL1 and FL2.
Insulation	1 layer of tape Item [6].
WD5 Shield2	Start with 4 strands of Item [4] and an excess of 20 mm as FL4 then wind 7 turns in 1 layer. Finish the winding at the right side and then cut the wire to leave it as No-Connect.
Insulation	1 layer of tape Item [6]
WD6 2nd Primary	Use hanging wire from WD1 and continue winding 17 turns from right to left and finish as FL4.
Insulation	1 layer of tape Item [6]
Finish	Bring 4 wires marked as FL1 to the right and secure with 2 layers of tape Item [6]. Insert Item [11] and Item [10] to FL3 and FL4 respectively. Gap cores to get 493 µH. Solder pin 4 with bus wire Item [9] then lean along the core halves. Secure by wrapping the body of the transformer with 2 layers of tape Item [7]. Use Item [8] to wrap both bottom secondary side halves of the exposed core as shown. Varnish using Item [12].



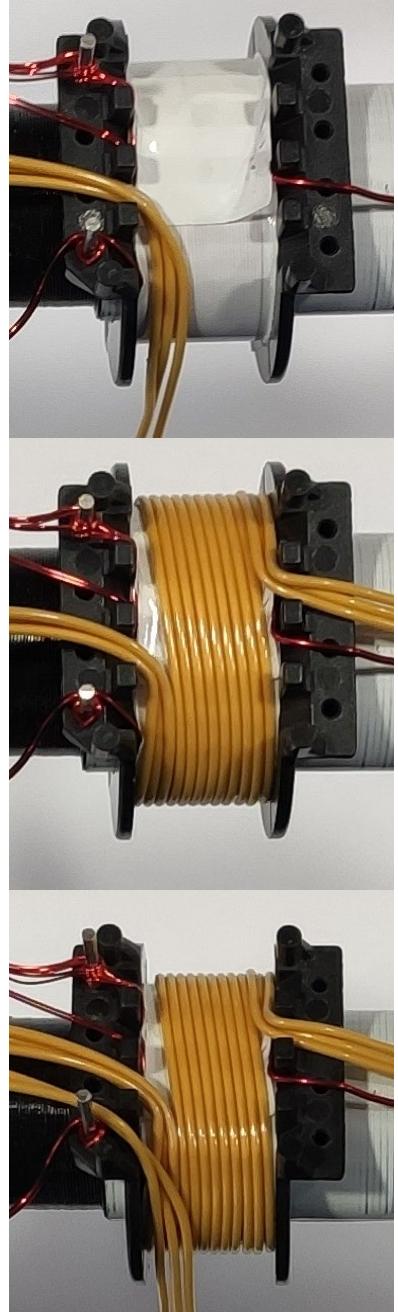
7.6 Transformer Winding Illustrations

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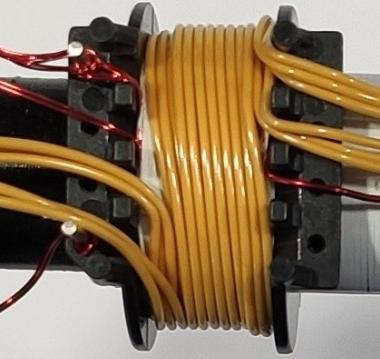
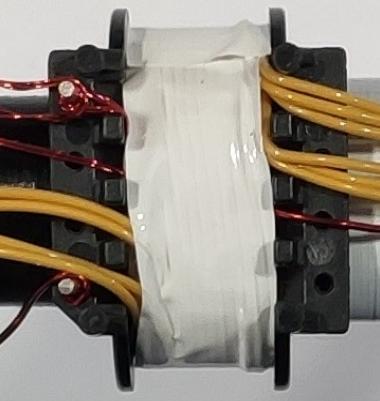
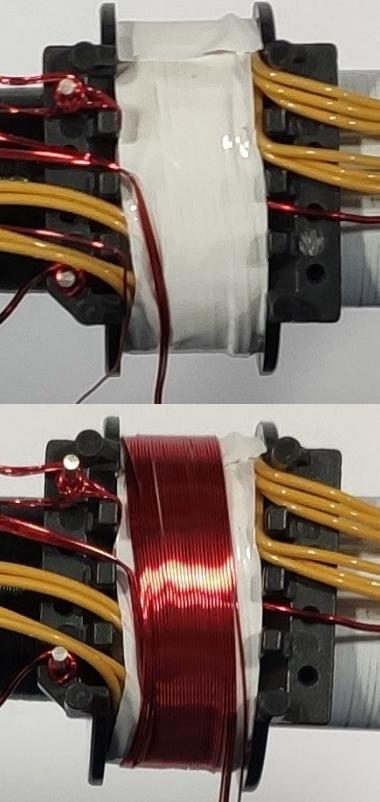


	 	
Insulation		1 layer of tape Item [6]

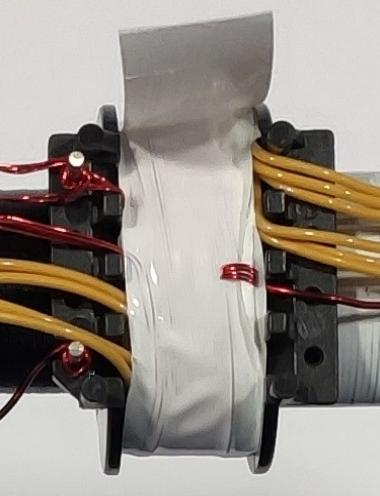
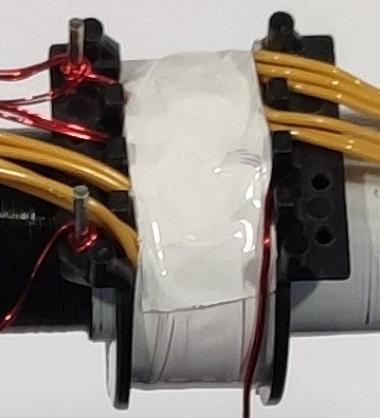
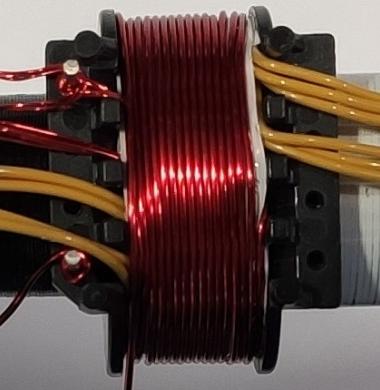
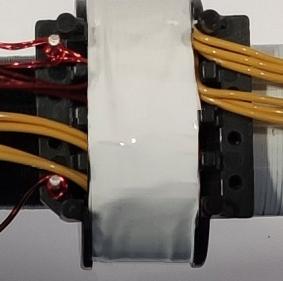


WD4 Secondary		<p>Start at left side of the bobbin. Use 3 wires Item [5], and leave ~25 mm length of excess wire, then mark as FL1. Wind 4 trifilar turns in 1 layer, from left to right, at the last turn exit the wires at right side of the bobbin, also leaving ~15 mm and mark FL2. Repeat the same winding above on top previous winding, also mark start and finish ends as FL1 and FL2.</p>
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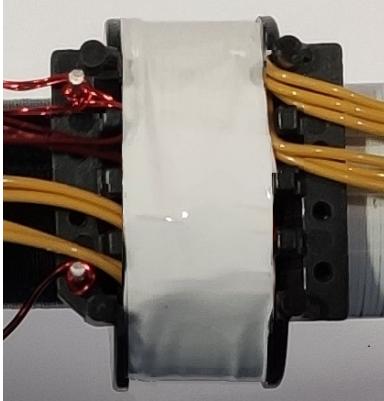
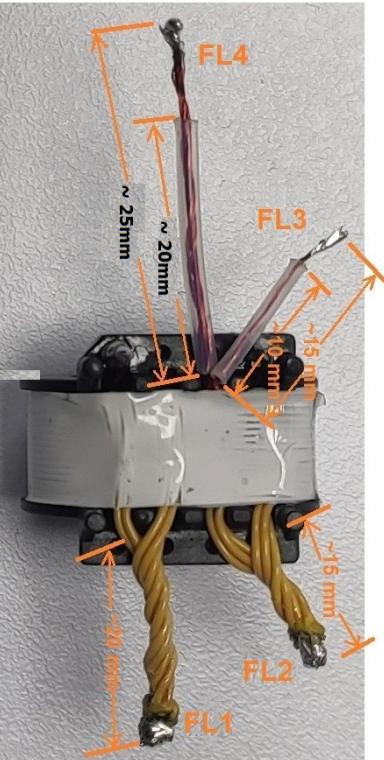


		
Insulation		1 layer of tape Item [6]
WD5 Shield2		Start with 4 strands of Item [4] and an excess of 20 mm as FL4 then wind 7 turns in 1 layer. Finish the winding at the right side and then cut the wire to leave it as No-Connect.

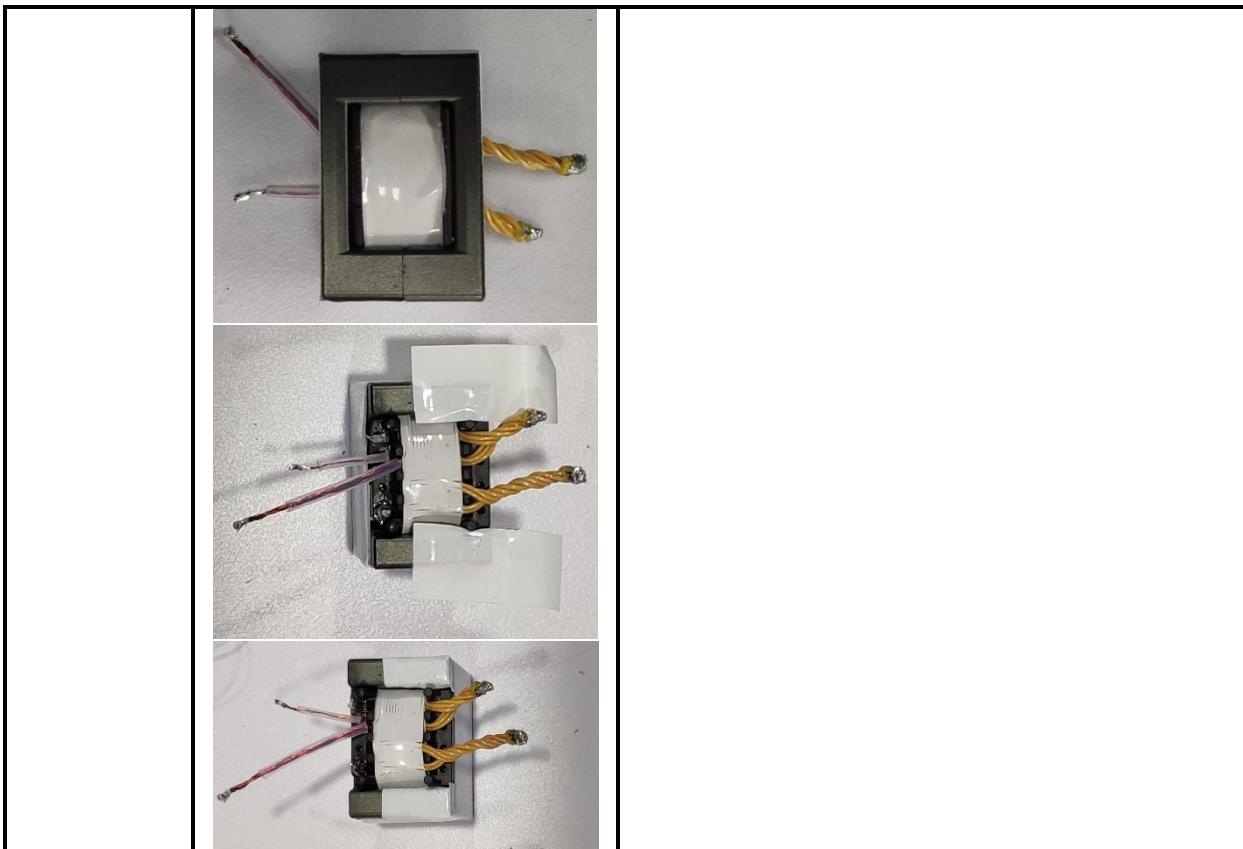


Insulation		1 layer of tape Item [6]
WD6 2nd Primary	 	Use hanging wire from WD1 and continue winding 17 turns from right to left and finish as FL4.
Insulation		1 layer of tape Item [6]



	  	
Finish	<p>Bring 4 wires marked as FL1 to the right and secure with 2 layers of tape Item [6]. Insert Item [11] and Item [10] to FL3 and FL4 respectively. Gap cores to get $493 \mu\text{H}$. Solder pin 4 with bus wire Item [9] then lean along the core halves. Secure by wrapping the body of the transformer with 2 layers of tape Item [7]. Use Item [8] to wrap both bottom secondary side halves of the exposed core as shown. Varnish using Item [12].</p>	





8 Design Spreadsheet

ACDC_InnoSwitch3-EP_Flyback_032521; Rev.1.7; Copyright Power Integrations 2021	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3 EP Flyback Design Spreadsheet
APPLICATION VARIABLES					
VIN_MIN	90		90	V	Minimum AC input voltage
VIN_MAX	440	Info	440	V	Input voltage too high: Decrease the maximum AC input voltage or verify the voltage rating of the input capacitor
VIN_RANGE			UNIVERSAL		Range of AC input voltage
LNEFREQ			60	Hz	AC Input voltage frequency
CAP_INPUT	104.0		104.0	uF	Input capacitor
VOUT	24.00		24.00	V	Output voltage at the board
CDC			0.00	mV	Cable drop compensation desired at full load
IOUT	2.500		2.500	A	Output current
POUT			60.00	W	Output power
EFFICIENCY	0.88		0.88		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
FACTOR_Z			0.50		Z-factor estimate
ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
PRIMARY CONTROLLER SELECTION					
ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
DEVICE_GENERIC	INN36X9		INN36X9		Generic device code
DEVICE_CODE			INN3679C		Actual device code
POUT_MAX			75	W	Power capability of the device based on thermal performance
RDS0N_100DEG			0.62	Ω	Primary switch on time drain resistance at 100 degC
ILIMIT_MIN			1.980	A	Minimum current limit of the primary switch
ILIMIT_TYP			2.130	A	Typical current limit of the primary switch
ILIMIT_MAX			2.279	A	Maximum current limit of the primary switch
VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
VDRAIN_ON_PRSW			0.44	V	Primary switch on time drain voltage
VDRAIN_OFF_PRSW		Warning*	890.9	V	The peak drain voltage on the switch is higher than 650V: Decrease the device VOR This design utilizes a 500V StackFET which increases the effective peak drain voltage capability to 1150V.
WORST CASE ELECTRICAL PARAMETERS					
FSWITCHING_MAX	75000		75000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
VOR	200.0		200.0	V	Secondary voltage reflected to the primary when the primary switch turns off
VMIN			89.78	V	Valley of the minimum input AC voltage at full load
KP			0.91		Measure of continuous/discontinuous mode of operation
MODE_OPERATION			CCM		Mode of operation
DUTYCYCLE			0.691		Primary switch duty cycle
TIME_ON			12.20	us	Primary switch on-time
TIME_OFF		Warning*	4.12	us	Primary switch off-time is shorter than 4.37us: Decrease the controller switching frequency or decrease the VOR Does not pose an issue as actual operating frequencies are well below the maximum operating frequency of 118 kHz.
LPRIMARY_MIN			468.0	uH	Minimum primary inductance
LPRIMARY_TYP			492.6	uH	Typical primary inductance



LPRIMARY_TOL			5.0	%	Primary inductance tolerance
LPRIMARY_MAX			517.3	uH	Maximum primary inductance
PRIMARY CURRENT					
IPEAK_PRIMARY			2.135	A	Primary switch peak current
IPEDESTAL_PRIMARY			0.178	A	Primary switch current pedestal
IAVG_PRIMARY			0.717	A	Primary switch average current
IRIPPLE_PRIMARY			2.135	A	Primary switch ripple current
IRMS_PRIMARY			1.010	A	Primary switch RMS current
SECONDARY CURRENT					
IPEAK_SECONDARY			18.147	A	Secondary winding peak current
IPEDESTAL_SECONDARY			1.517	A	Secondary winding current pedestal
IRMS_SECONDARY			5.740	A	Secondary winding RMS current
TRANSFORMER CONSTRUCTION PARAMETERS					
CORE SELECTION					
CORE	ATQ25/16	Info	ATQ25/16		Refer to the Transformer Parameters tab to verify fit factor
CORE CODE			ATQ25/16		Core code
AE			102.00	mm^2	Core cross sectional area
LE			40.80	mm	Core magnetic path length
AL			6700	nH/turns^2	Ungapped core effective inductance
VE			4162.0	mm^3	Core volume
BOBBIN			TBI-238-09011.11XX		Bobbin
AW			25.60	mm^2	Window area of the bobbin
BW			8.00	mm	Bobbin width
MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
PRIMARY WINDING					
NPRIMARY			34		Primary turns
BPEAK			3479	Gauss	Peak flux density
BMAX			3143	Gauss	Maximum flux density
BAC			1571	Gauss	AC flux density (0.5 x Peak to Peak)
ALG			426	nH/turns^2	Typical gapped core effective inductance
LG			0.282	mm	Core gap length
LAYERS_PRIMARY	2		2		Number of primary layers
AWG_PRIMARY			26	AWG	Primary winding wire AWG
OD_PRIMARY_INSULATED			0.465	mm	Primary winding wire outer diameter with insulation
OD_PRIMARY_BARE			0.405	mm	Primary winding wire outer diameter without insulation
CMA_PRIMARY			251	Cmil/A	Primary winding wire CMA
SECONDARY WINDING					
NSECONDARY	4		4		Secondary turns
AWG_SECONDARY			19	AWG	Secondary winding wire AWG
OD_SECONDARY_INSULATED			1.217	mm	Secondary winding wire outer diameter with insulation
OD_SECONDARY_BARE			0.912	mm	Secondary winding wire outer diameter without insulation
CMA_SECONDARY			224	Cmil/A	Secondary winding wire CMA
BIAS WINDING					
NBIAS			2		Bias turns
PRIMARY COMPONENTS SELECTION					
LINE UNDERTVOLTAGE					
BROWN-IN REQUIRED			72.0	V	Required AC RMS line voltage brown-in threshold
RLS			3.64	MΩ	Connect two 1.82 MΩ resistors to the V-pin for the required UV/OV threshold
BROWN-IN ACTUAL			73.0	V	Actual AC RMS brown-in threshold
BROWN-OUT ACTUAL			66.0	V	Actual AC RMS brown-out threshold
LINE OVERVOLTAGE					
OVERVOLTAGE_LINE		Warning*	304.2	V	The device voltage stress will be higher than 650V when overvoltage is triggered



					This design utilizes a 500V StackFET which increases the effective peak drain voltage capability to 1150V.
BIAS DIODE					
VBIAS	10.0		10.0	V	Rectified bias voltage
VF_BIAS			0.70	V	Bias winding diode forward drop
VREVERSE_BIASDIODE			46.52	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
CBIAS			22	uF	Bias winding rectification capacitor
CBPP			4.70	uF	BPP pin capacitor
SECONDARY COMPONENTS					
RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
RFB_LOWER			5.62	kΩ	Lower feedback resistor
CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
OUTPUT PARAMETERS					
VOUT			24.00	V	Output 1 voltage
IOUT			2.50	A	Output 1 current
POUT			60.00	W	Output 1 power
IRMS_SECONDARY			5.740	A	Root mean squared value of the secondary current for output 1
IRIPPLE_CAP_OUTPUT			5.168	A	Current ripple on the secondary waveform for output 1
AWG_SECONDARY			19	AWG	Wire size for output 1
OD_SECONDARY_INSULATED			1.217	mm	Secondary winding wire outer diameter with insulation for output 1
OD_SECONDARY_BARE			0.912	mm	Secondary winding wire outer diameter without insulation for output 1
CM_SECONDARY			1148	Cmils	Bare conductor effective area in circular mils for output 1
NSECONDARY			4		Number of turns for output 1
VREVERSE_RECTIFIER			97.04	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
SRFET	AUTO		AON7254		Secondary rectifier (Logic MOSFET) for output 1
VF_SRFET			0.165	V	SRFET on-time drain voltage for output 1
VBREAKDOWN_SRFET			150	V	SRFET breakdown voltage for output 1
RDSON_SRFET			66.0	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1

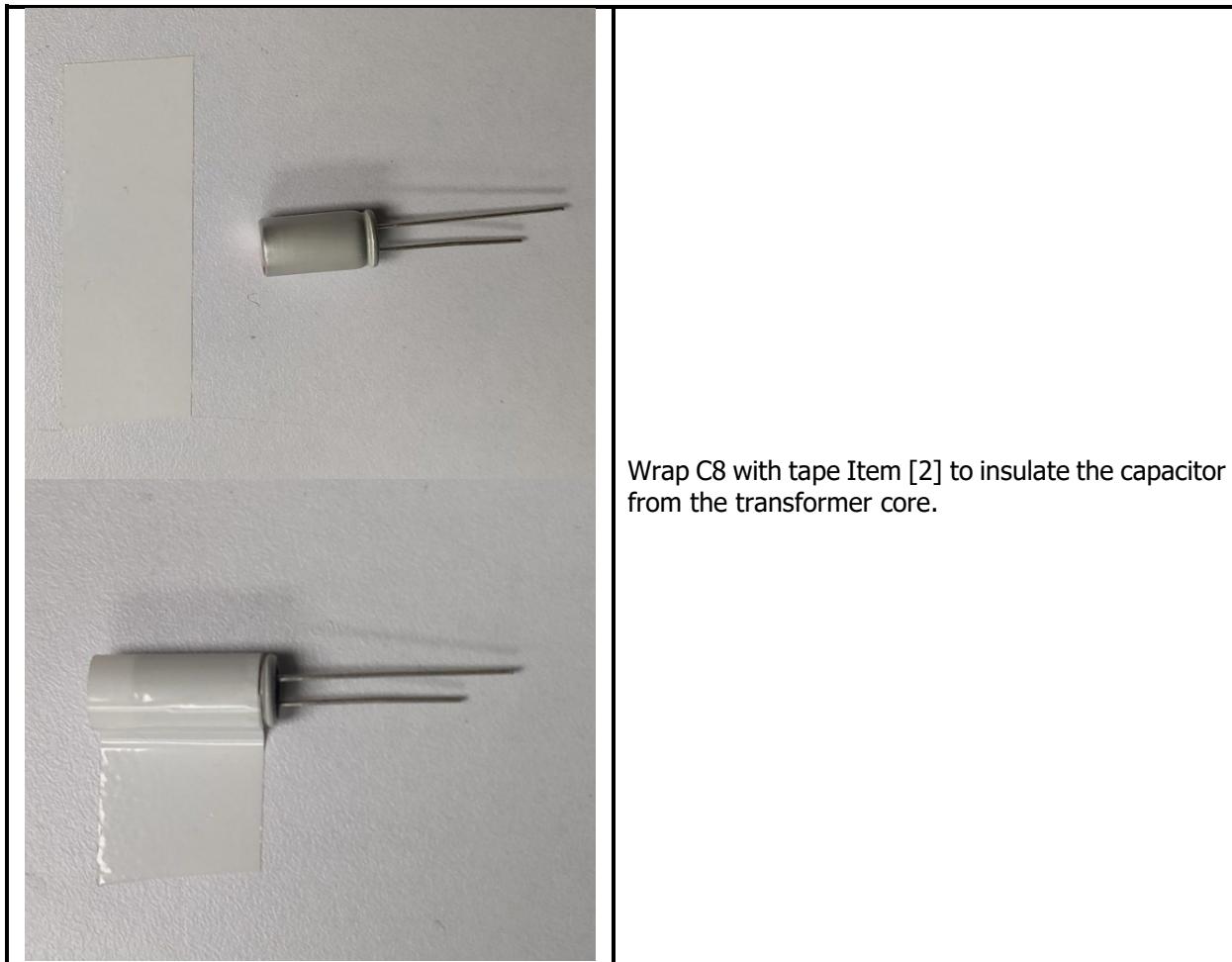


9 PCB Assembly Instructions

9.1 Materials

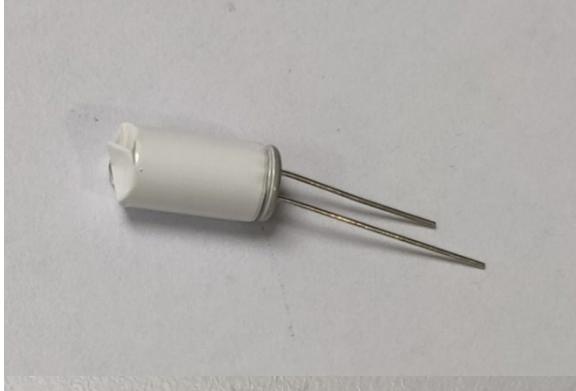
Item	Description
[1]	Capacitor C8.
[2]	Polyester Tape: 20 mm X 40 mm.
[3]	Polyester Tape: 5 mm X 20 mm.
[4]	Resistor R3.
[5]	AWG #24 PTFE Non-Shrink Tubing 12 mm.

9.2 Components Assembly Instructions



Wrap C8 with tape Item [2] to insulate the capacitor from the transformer core.



	
	Fold the tape on top of the capacitor and secure using Item [3].
	
	Insert Item [5] into the resistor (R3).



	<p>Solder the assemble C8, and R3 to PCB.</p> <p>Please take note on the polarity of the electrolytic capacitor C8 during insertion to the PCB.</p> <p>Finish assembly.</p>

Note: Cut all the TH pins to <0.5 mm on the bottom side of the board after completing the assembly.



10 Performance Data

10.1 Efficiency

10.1.1 Average Efficiency

10.1.1.1 90 VAC / 60 Hz

Load (A)	V _{IN} (V _{RMS})	I _{IN} (mA _{RMS})	P _{IN} (W)	V _{OUT} at PCB (V _{Dc})	I _{OUT} (mA _{Dc})	P _{OUT} (W)	Efficiency at PCB (%)
100%	90	912.7	64.35	23.24	2499.20	58.09	90.27
75%	90	689.30	48.39	23.48	1874.30	44.01	90.94
50%	90	468.90	32.28	23.60	1249.60	29.49	91.34
25%	90	247.31	16.18	23.65	624.80	14.78	91.31
						Average	90.97

10.1.1.2 115 VAC / 60 Hz

Load (A)	V _{IN} (V _{RMS})	I _{IN} (mA _{RMS})	P _{IN} (W)	V _{OUT} at PCB (V _{Dc})	I _{OUT} (mA _{Dc})	P _{OUT} (W)	Efficiency at PCB (%)
100%	115	740.60	63.93	23.43	2499.30	58.57	91.61
75%	115	564.70	48.01	23.55	1874.40	44.14	91.94
50%	115	387.50	32.03	23.61	1249.70	29.50	92.11
25%	115	207.03	16.11	23.65	624.80	14.78	91.75
						Average	91.85

10.1.1.3 230 VAC / 50 Hz

Load (A)	V _{IN} (V _{RMS})	I _{IN} (mA _{RMS})	P _{IN} (W)	V _{OUT} at PCB (V _{Dc})	I _{OUT} (mA _{Dc})	P _{OUT} (W)	Efficiency at PCB (%)
100%	230	454.10	64.07	23.52	2499.30	58.77	91.73
75%	230	346.50	48.18	23.58	1874.40	44.19	91.72
50%	230	239.14	32.28	23.61	1249.70	29.51	91.41
25%	230	129.60	16.42	23.63	624.80	14.76	89.91
						Average	91.19

10.1.1.4 300 VAC / 50 Hz

Load (A)	V _{IN} (V _{RMS})	I _{IN} (mA _{RMS})	P _{IN} (W)	V _{OUT} at PCB (V _{Dc})	I _{OUT} (mA _{Dc})	P _{OUT} (W)	Efficiency at PCB (%)
100%	300	362.14	64.56	23.52	2499.30	58.78	91.05
75%	300	279.51	48.63	23.58	1874.40	44.19	90.87
50%	300	195.11	32.69	23.61	1249.70	29.50	90.25
25%	300	107.50	16.77	23.62	624.80	14.76	88.01
						Average	90.05



10.1.1.5 350 VAC / 50 Hz

Load (A)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	Efficiency at PCB (%)
100%	350	320.35	64.92	23.53	2499.30	58.82	90.60
75%	350	248.10	48.94	23.58	1874.40	44.19	90.29
50%	350	173.97	32.96	23.61	1249.70	29.51	89.52
25%	350	96.64	16.96	23.61	624.80	14.75	86.96
						Average	89.35

10.1.1.6 440 VAC / 50 Hz

Load (A)	V_{IN} (V_{RMS})	I_{IN} (mA_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} (mA_{DC})	P_{OUT} (W)	Efficiency at PCB (%)
100%	440	267.29	65.16	23.55	2499.30	58.86	90.33
75%	440	207.77	49.14	23.59	1874.40	44.21	89.98
50%	440	146.40	33.13	23.62	1249.70	29.51	89.09
25%	440	82.32	17.10	23.61	624.80	14.75	86.26
						Average	88.92



10.1.2 Full Load Efficiency vs. Line

Test Condition: Soak for 5 minutes for each line.

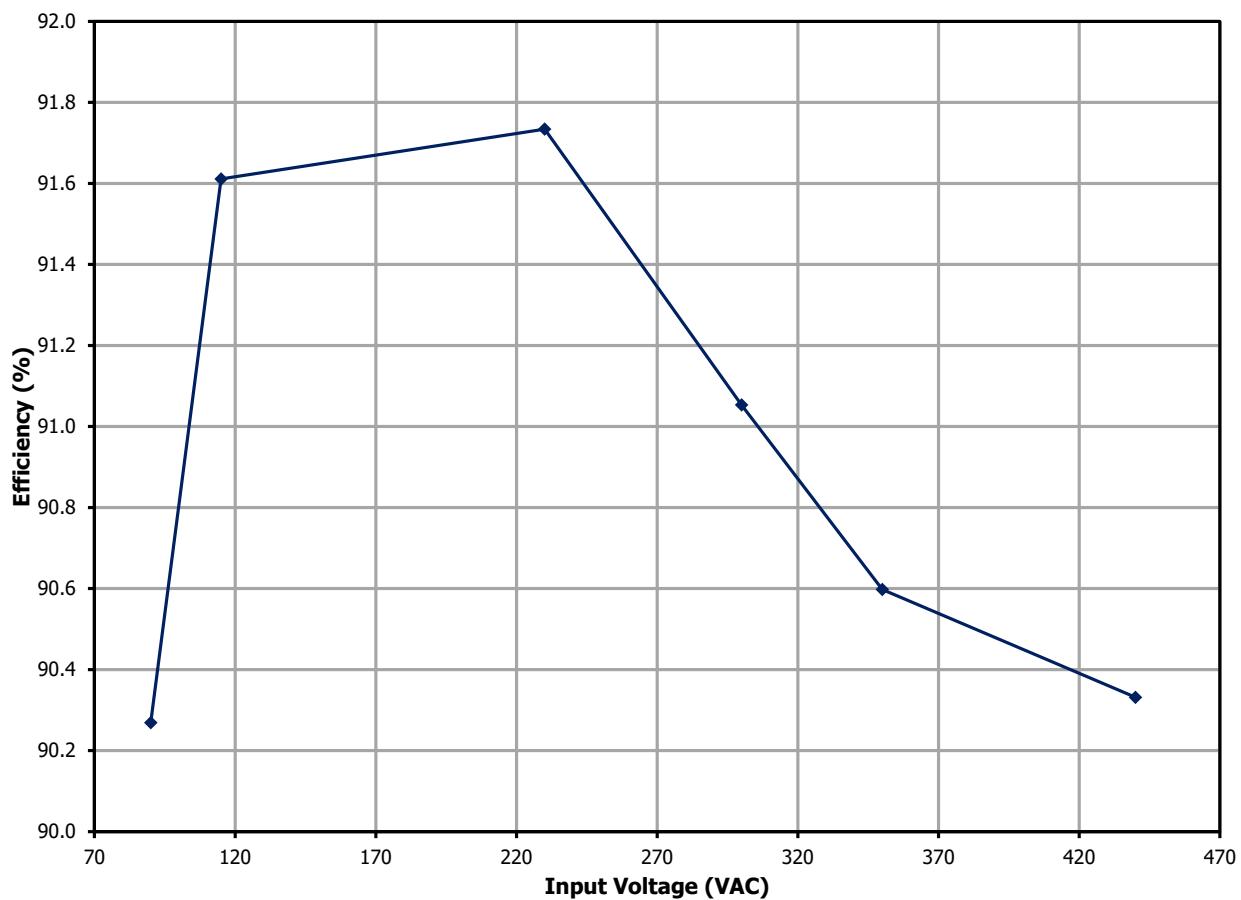


Figure 8 – Full Load Efficiency vs. Line.



10.1.3 Efficiency vs. Load

Test Condition: Soak for 5 minutes each line, and 30 seconds for each load.

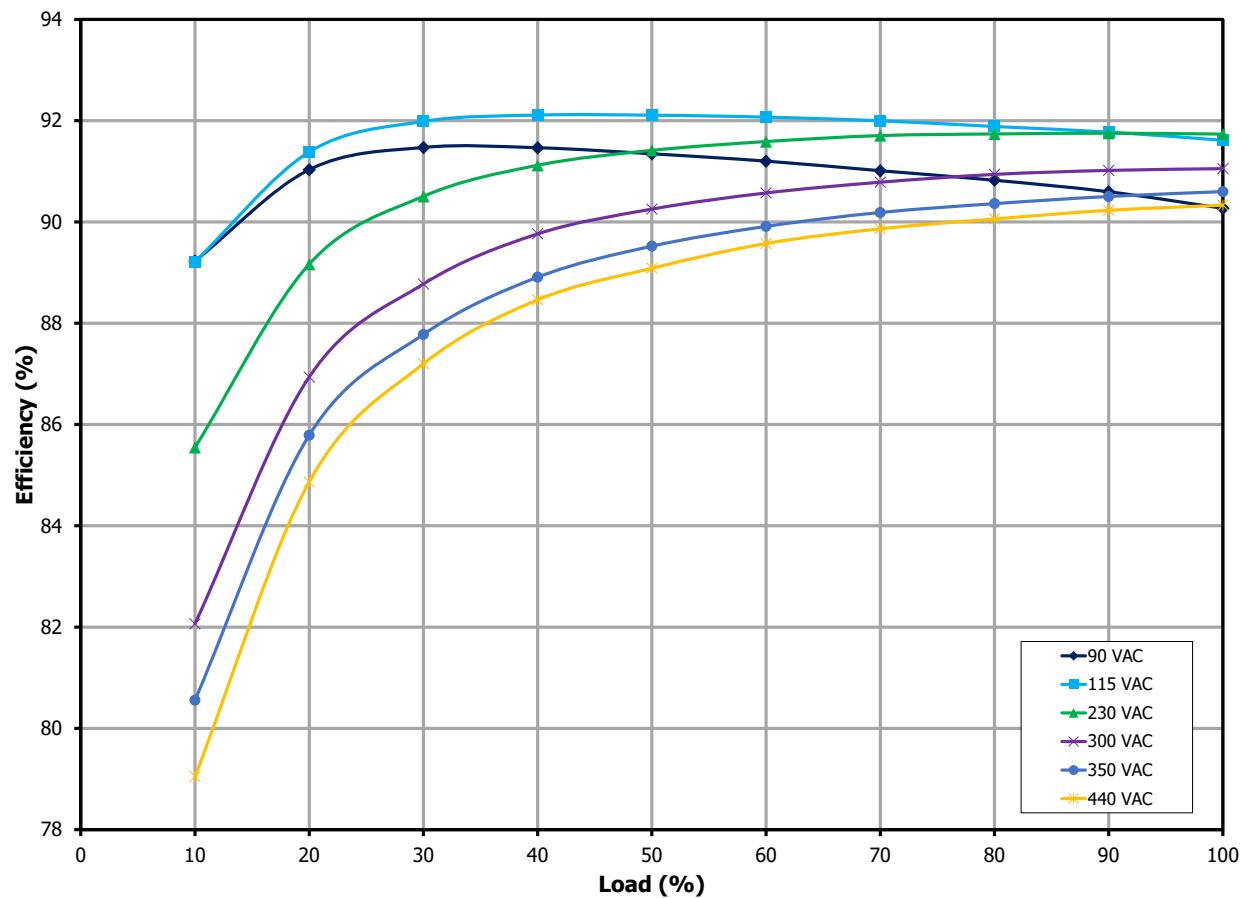


Figure 9 – Efficiency vs. Percentage Load.

10.2 Available Standby Output Power

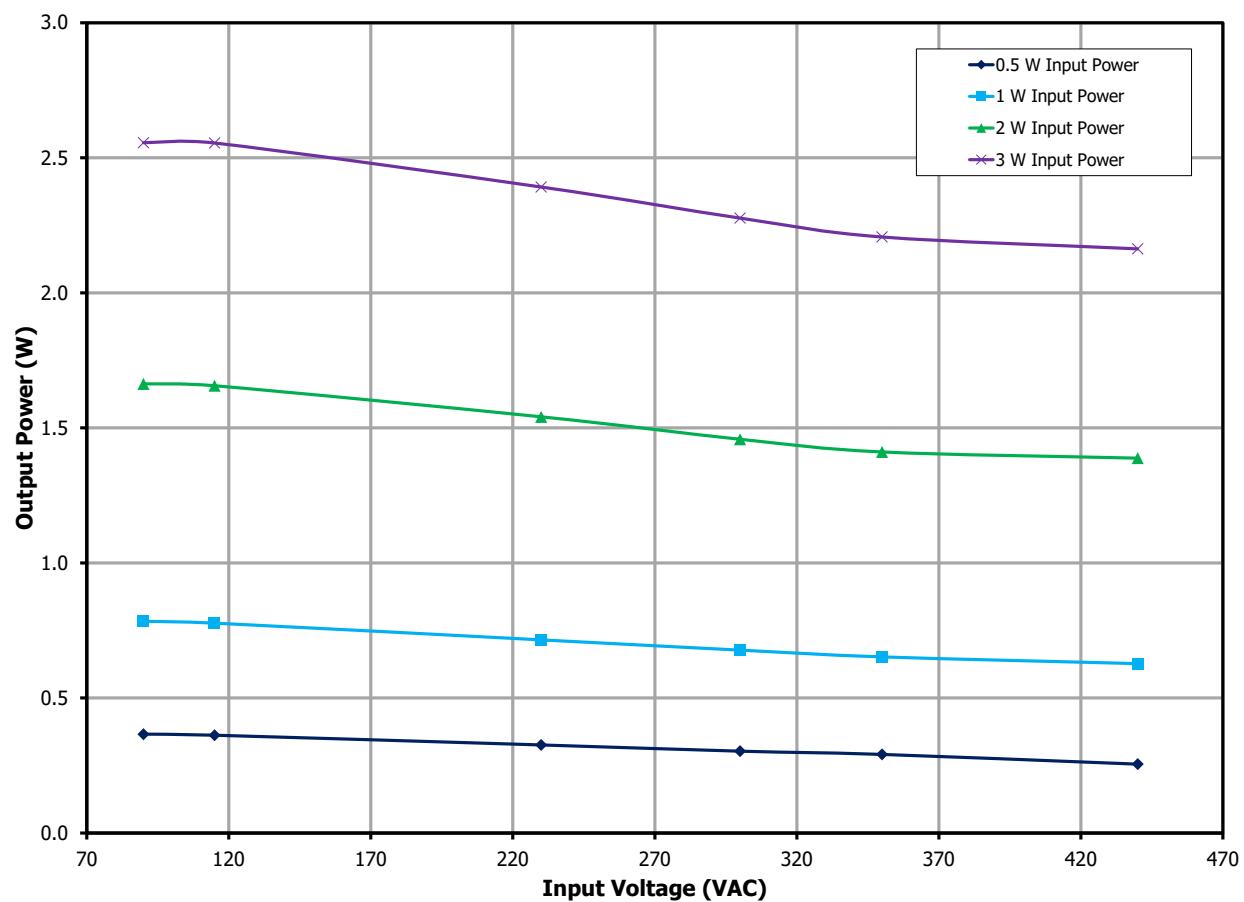


Figure 10 – Available Standby Output Power for 0.5 W, 1 W, 2 W and 3 W Input Power.

10.3 No-Load Input Power

Test Condition: Soak for 5 minutes each line and 2-minute integration time.

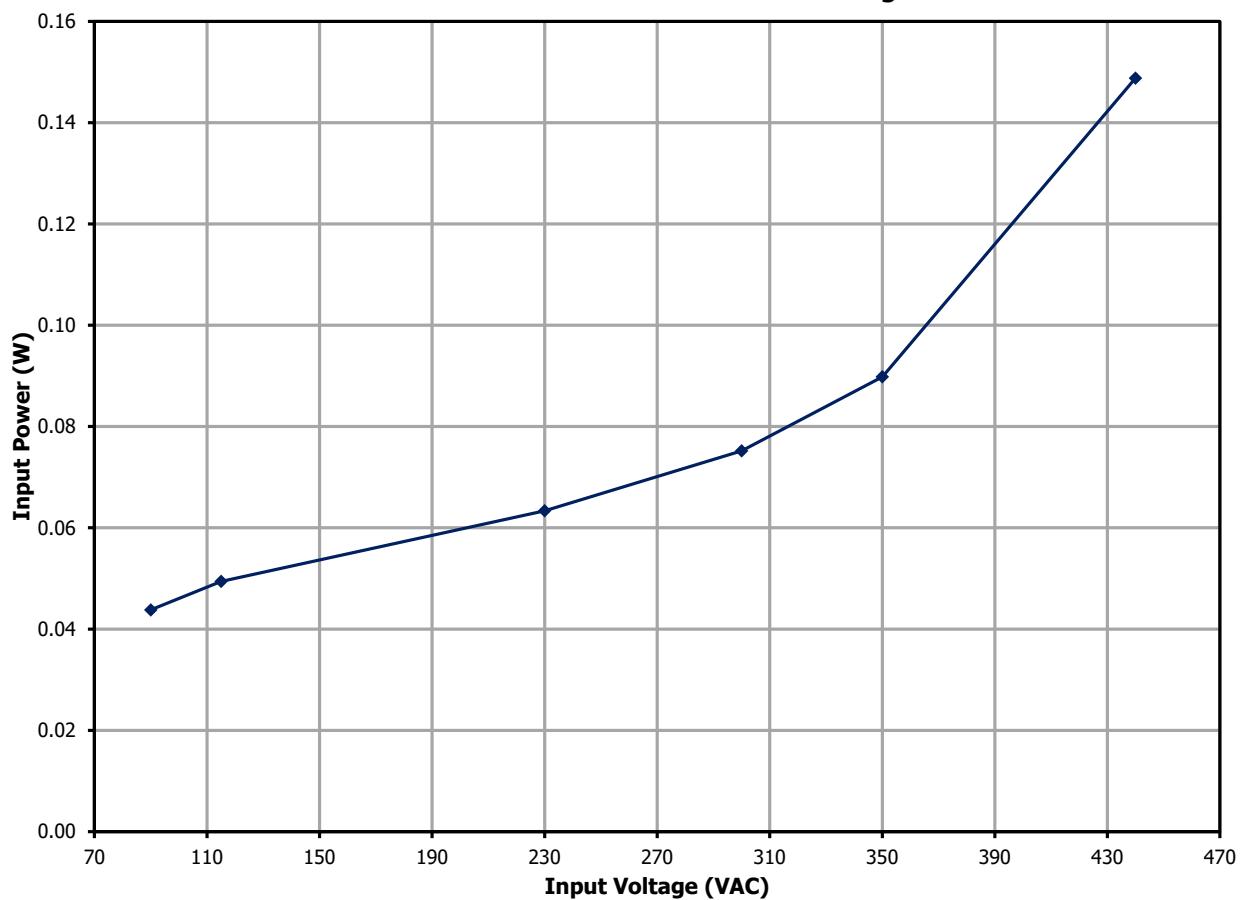


Figure 11 – No-Load Input Power vs. Line at Room Temperature.



10.4 Line Regulation

Test Condition: Soak for 5 minutes for each line.

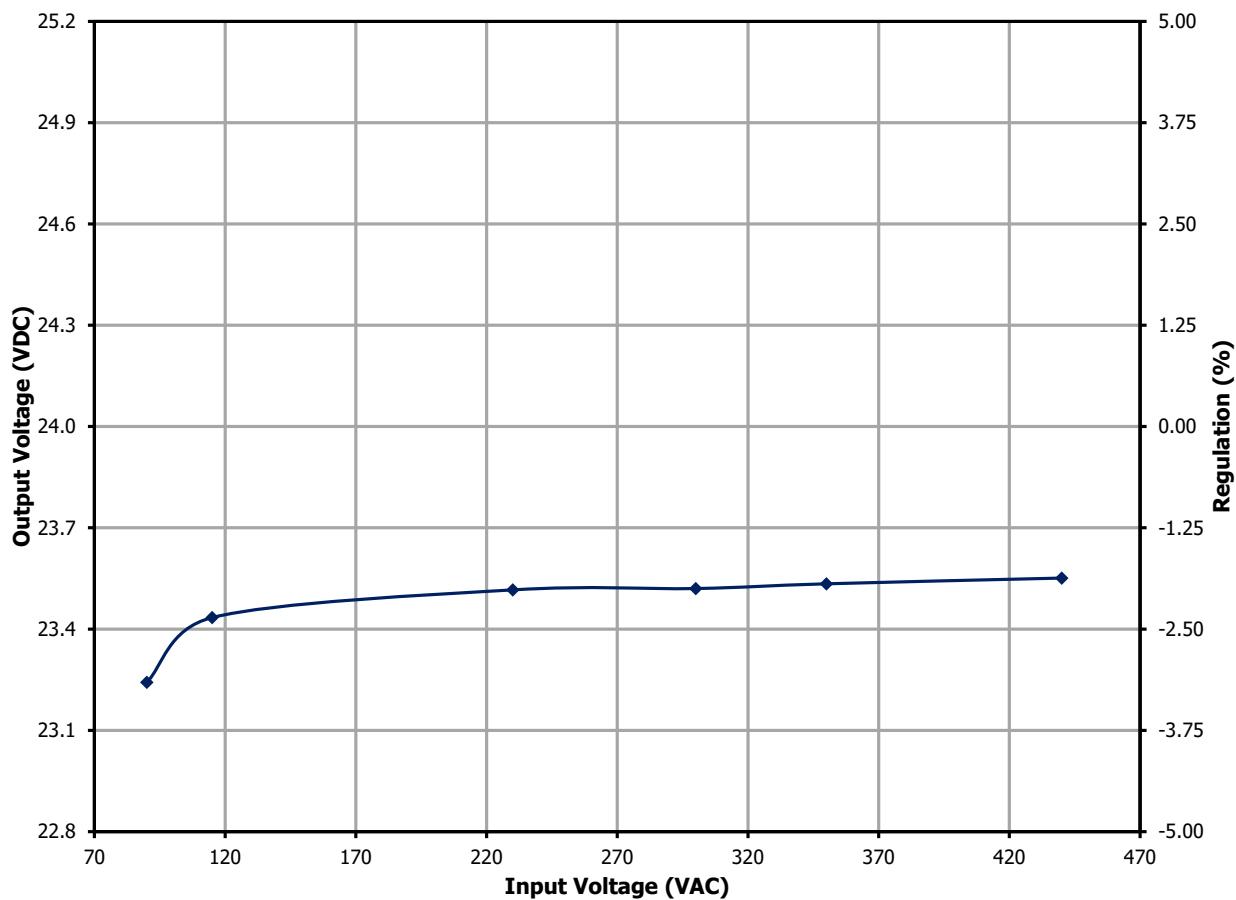


Figure 12 – Output Voltage vs. Line Voltage.



10.5 Load Regulation

Test Condition: Soak for 5 minutes each line, and 30 seconds for each load.

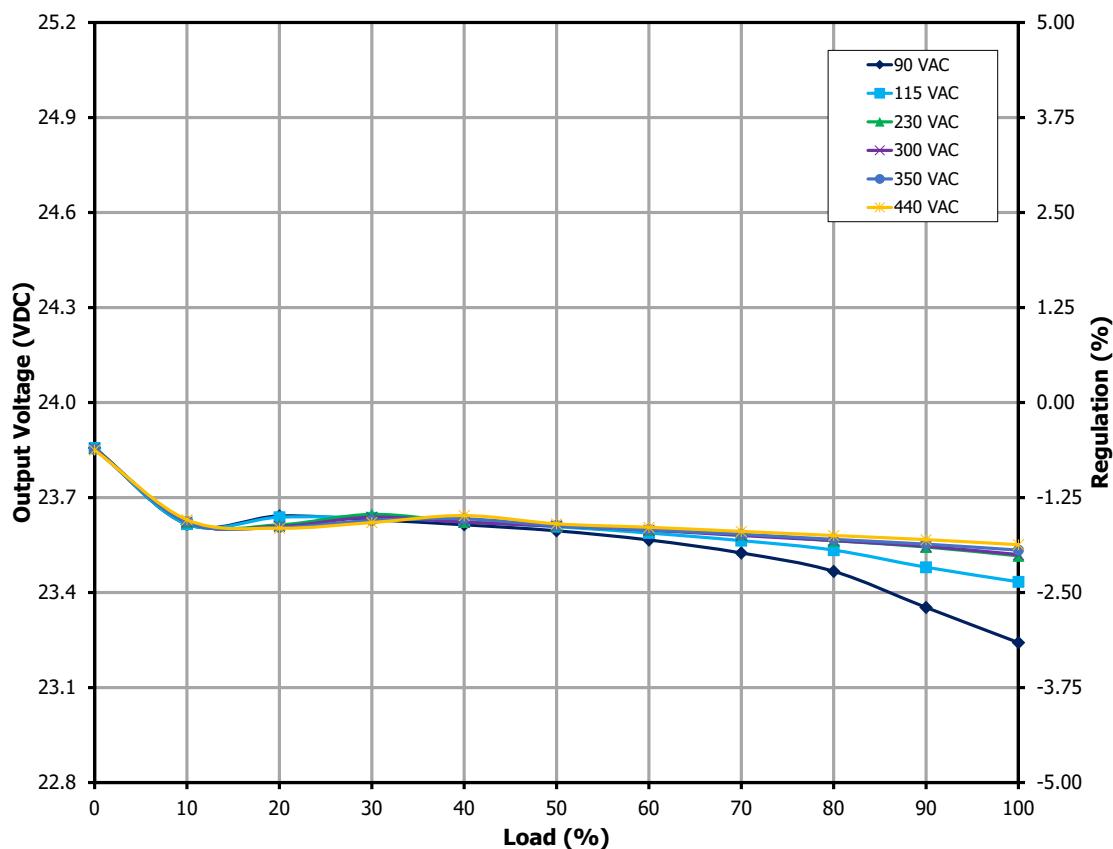


Figure 13 – Output Voltage vs. Percent Load.



11 Waveforms

11.1 Load Transient Response

Test Condition: Frequency = 500 Hz, Duty cycle = 50 %, Slew Rate = 800 mA / μ s

11.1.1 0% - 100% Load Change

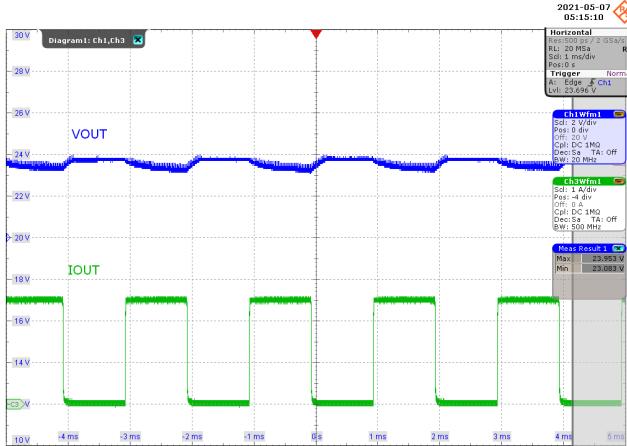


Figure 14 – 90 VAC 60 Hz.

CH1: VOUT, 2 V / div., 1 ms / div.
CH3: IOUT, 1 A / div., 1 ms / div.
 V_{MAX} : 23.95 V, V_{MIN} : 23.08 V.

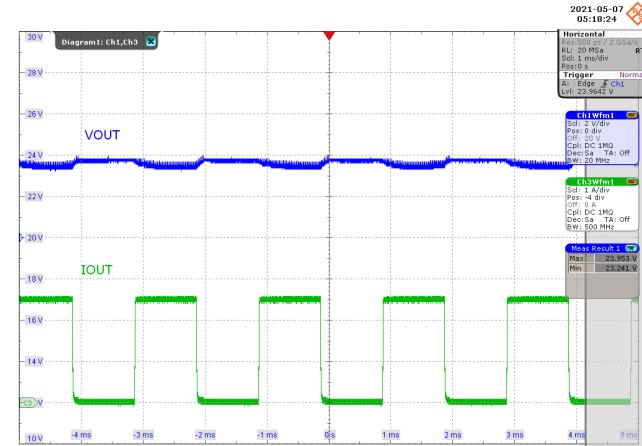


Figure 15 – 115 VAC 60 Hz.

CH1: VOUT, 2 V / div., 1 ms / div.
CH3: IOUT, 1 A / div., 1 ms / div.
 V_{MAX} : 23.95 V, V_{MIN} : 23.24 V.

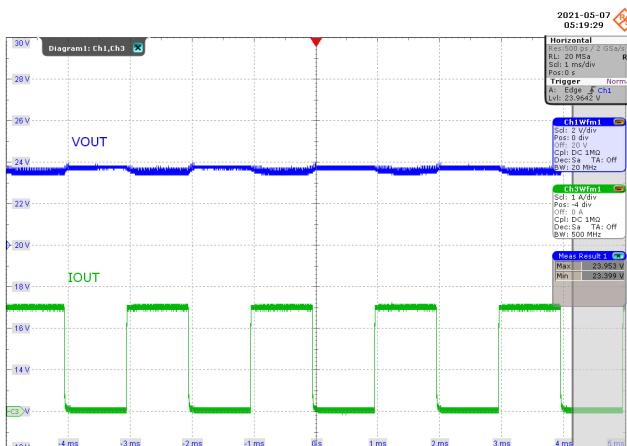


Figure 16 – 230 VAC 60 Hz.

CH1: VOUT, 2 V / div., 1 ms / div.
CH3: IOUT, 1 A / div., 1 ms / div.
 V_{MAX} : 23.95 V, V_{MIN} : 23.40 V.

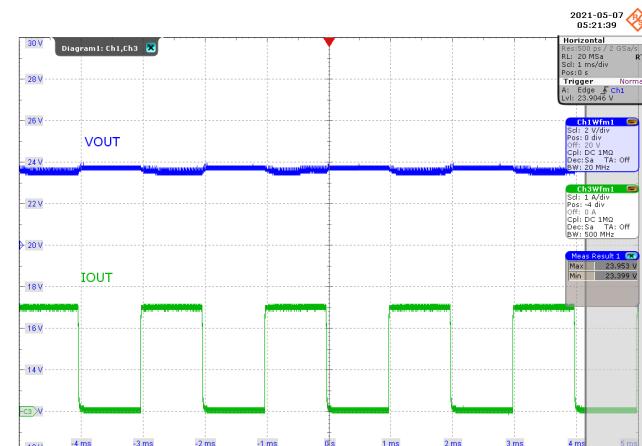
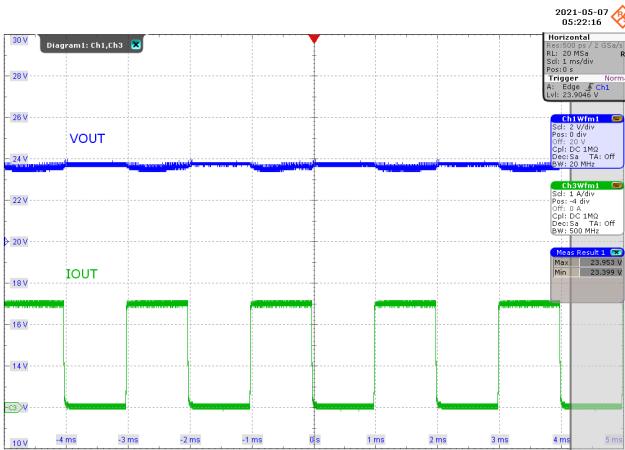


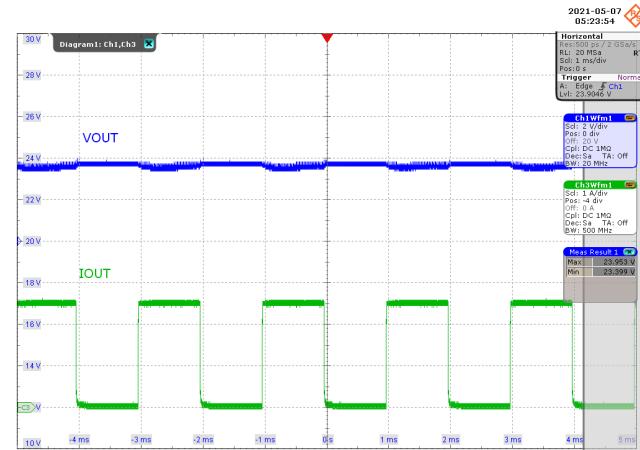
Figure 17 – 300 VAC 60 Hz.

CH1: VOUT, 2 V / div., 1 ms / div.
CH3: IOUT, 1 A / div., 1 ms / div.
 V_{MAX} : 23.95 V, V_{MIN} : 23.40 V.



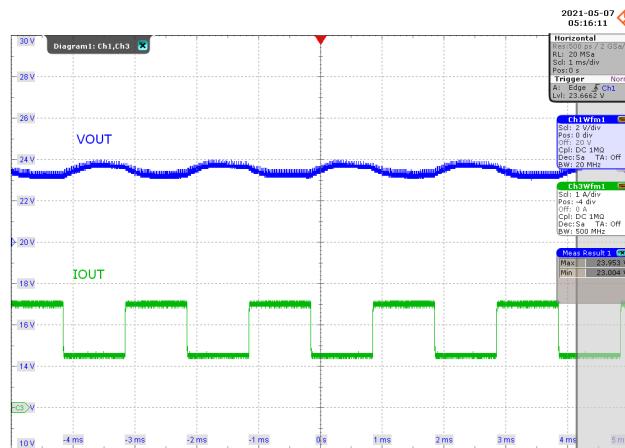
**Figure 18 – 350 VAC 60 Hz.**

CH1: V_{OUT}, 2 V / div., 1 ms / div.
CH3: I_{OUT}, 1 A / div., 1 ms / div.
V_{MAX}: 23.95 V, V_{MIN}: 23.40 V.

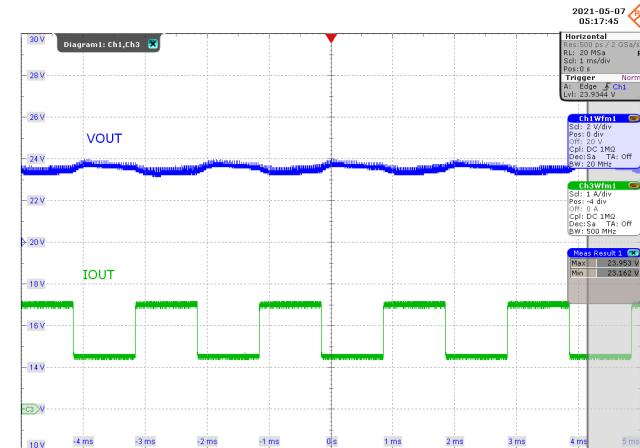
**Figure 19 – 440 VAC 60 Hz.**

CH1: V_{OUT}, 2 V / div., 1 ms / div.
CH3: I_{OUT}, 1 A / div., 1 ms / div.
V_{MAX}: 23.95 V, V_{MIN}: 23.40 V.

11.1.2 50% - 100% Load Change

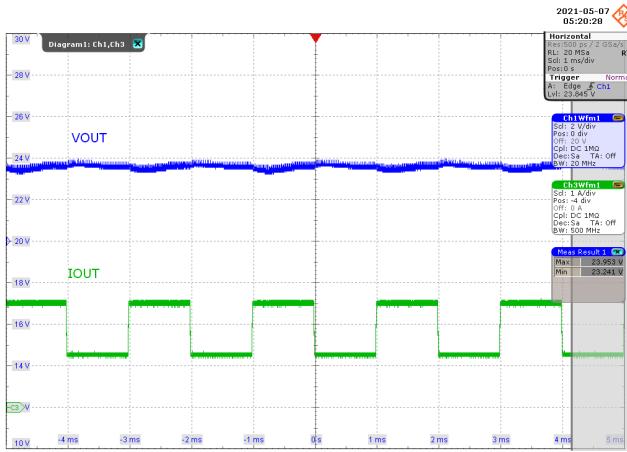
**Figure 20 – 90 VAC 60 Hz.**

CH1: V_{OUT}, 2 V / div., 1 ms / div.
CH3: I_{OUT}, 1 A / div., 1 ms / div.
V_{MAX}: 23.95 V, V_{MIN}: 23.00 V.

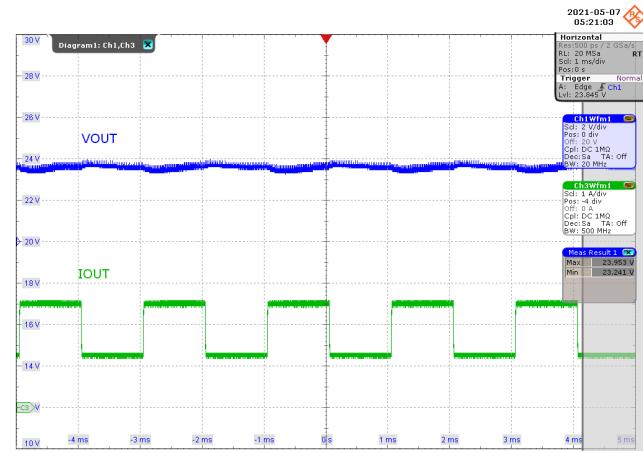
**Figure 21 – 115 VAC 60 Hz.**

CH1: V_{OUT}, 2 V / div., 1 ms / div.
CH3: I_{OUT}, 1 A / div., 1 ms / div.
V_{MAX}: 23.95 V, V_{MIN}: 23.16 V.

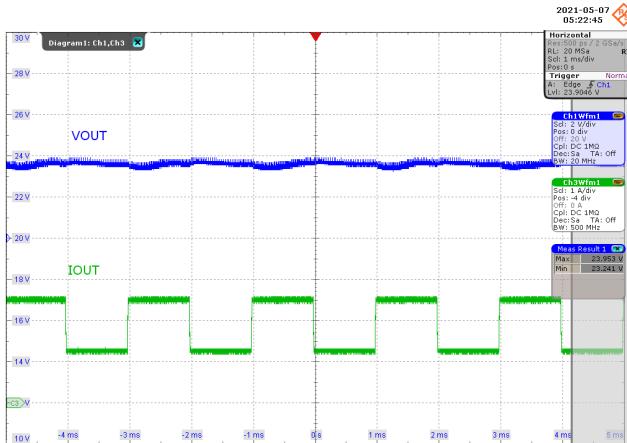


**Figure 22 – 230 VAC 60 Hz.**

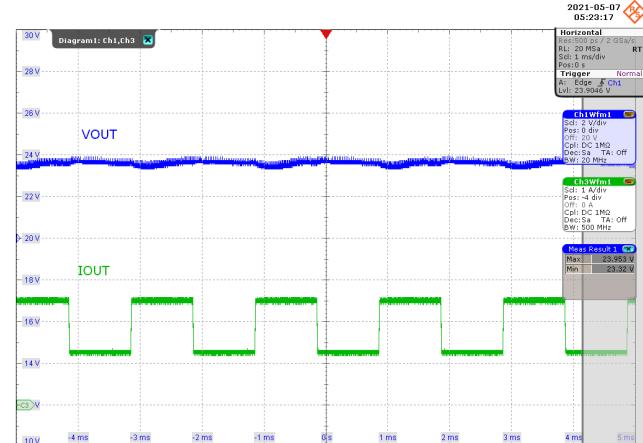
CH1: V_{OUT}, 2 V / div., 1 ms / div.
 CH3: I_{OUT}, 1 A / div., 1 ms / div.
 V_{MAX}: 23.95 V, V_{MIN}: 23.24 V.

**Figure 23 – 300 VAC 60 Hz.**

CH1: V_{OUT}, 2 V / div., 1 ms / div.
 CH3: I_{OUT}, 1 A / div., 1 ms / div.
 V_{MAX}: 23.95 V, V_{MIN}: 23.24 V.

**Figure 24 – 350 VAC 60 Hz.**

CH1: V_{OUT}, 2 V / div., 1 ms / div.
 CH3: I_{OUT}, 1 A / div., 1 ms / div.
 V_{MAX}: 23.95 V, V_{MIN}: 23.24 V.

**Figure 25 – 440 VAC 60 Hz.**

CH1: V_{OUT}, 2 V / div., 1 ms / div.
 CH3: I_{OUT}, 1 A / div., 1 ms / div.
 V_{MAX}: 23.95 V, V_{MIN}: 23.32 V.



11.2 Output Voltage at Start-up

11.2.1 CC Mode

11.2.1.1 100% Load

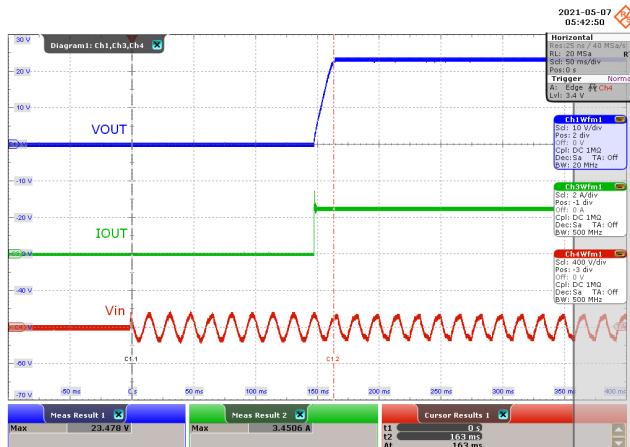


Figure 26 – 90 VAC 60 Hz.

CH1: V_{OUT}, 10 V / div., 50 ms / div.

CH3: I_{OUT}, 2 A / div., 50 ms / div.

CH4: V_{IN}, 400 V / div., 50 ms / div.

On-Time Delay = 163 ms.

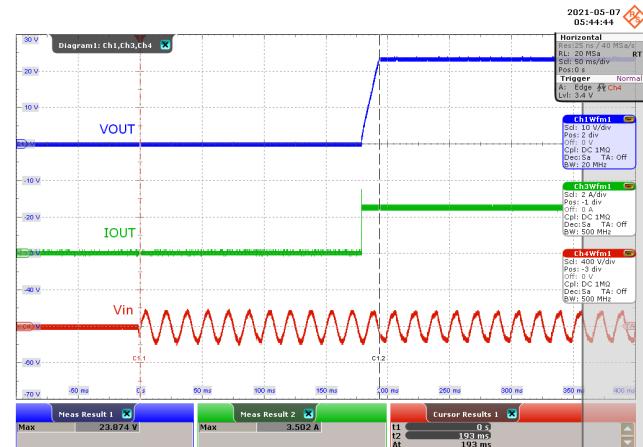


Figure 27 – 115 VAC 60 Hz.

CH1: V_{OUT}, 10 V / div., 50 ms / div.

CH3: I_{OUT}, 2 A / div., 50 ms / div.

CH4: V_{IN}, 400 V / div., 50 ms / div.

On-Time Delay = 193 ms.

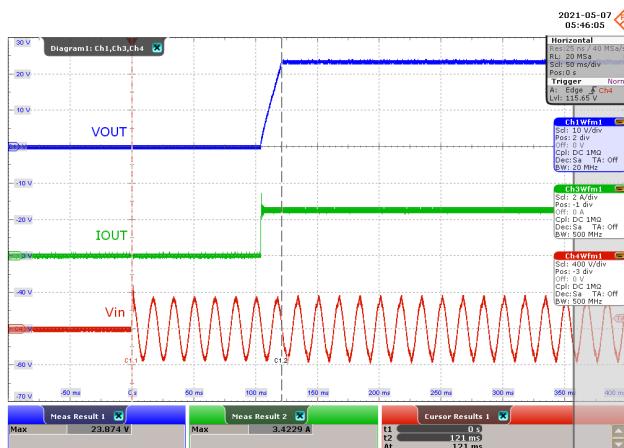


Figure 28 – 230 VAC 60 Hz.

CH1: V_{OUT}, 10 V / div., 50 ms / div.

CH3: I_{OUT}, 2 A / div., 50 ms / div.

CH4: V_{IN}, 400 V / div., 50 ms / div.

On-Time Delay = 121 ms.

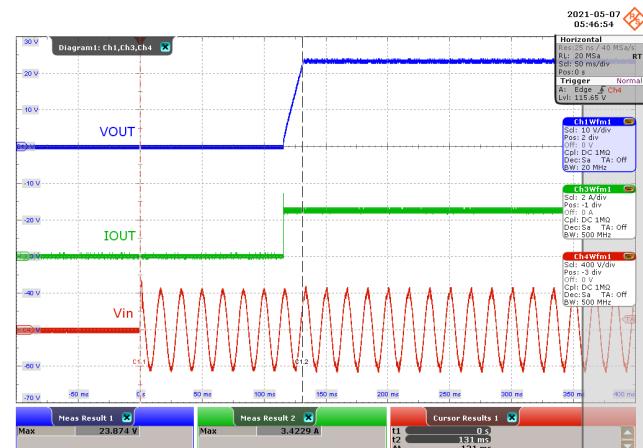


Figure 29 – 300 VAC 60 Hz.

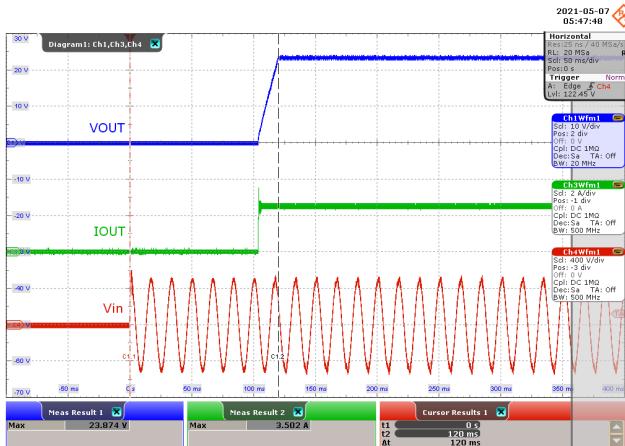
CH1: V_{OUT}, 10 V / div., 50 ms / div.

CH3: I_{OUT}, 2 A / div., 50 ms / div.

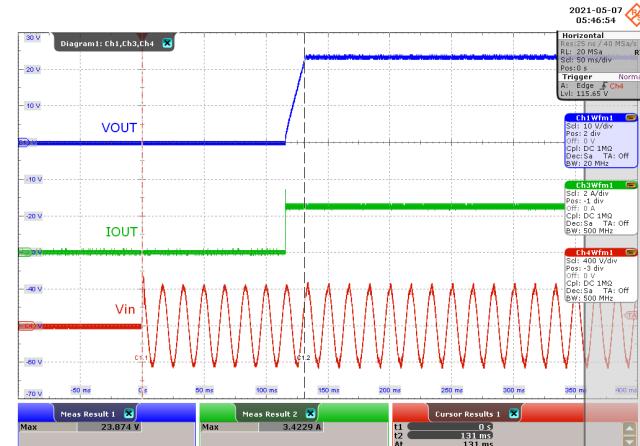
CH4: V_{IN}, 400 V / div., 50 ms / div.

On-Time Delay = 131 ms.



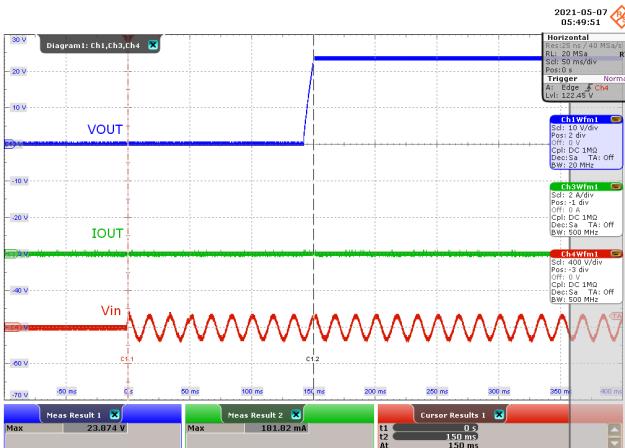
**Figure 30 – 350 VAC 60 Hz.**CH1: V_{OUT}, 10 V / div., 50 ms / div.CH3: I_{OUT}, 2 A / div., 50 ms / div.CH4: V_{IN}, 400 V / div., 50 ms / div.

On-Time Delay = 120 ms.

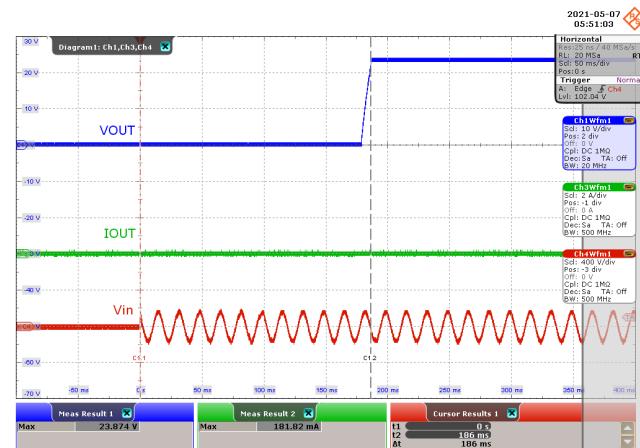
**Figure 31 – 440 VAC 60 Hz.**CH1: V_{OUT}, 10 V / div., 50 ms / div.CH3: I_{OUT}, 2 A / div., 50 ms / div.CH4: V_{IN}, 400 V / div., 50 ms / div.

On-Time Delay = 131 ms.

11.2.1.2 0% Load

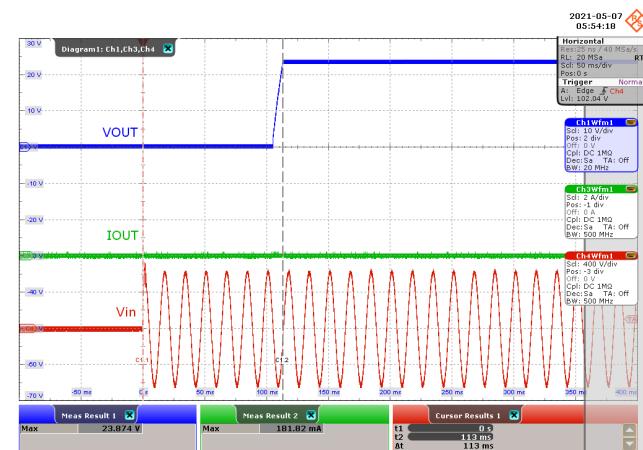
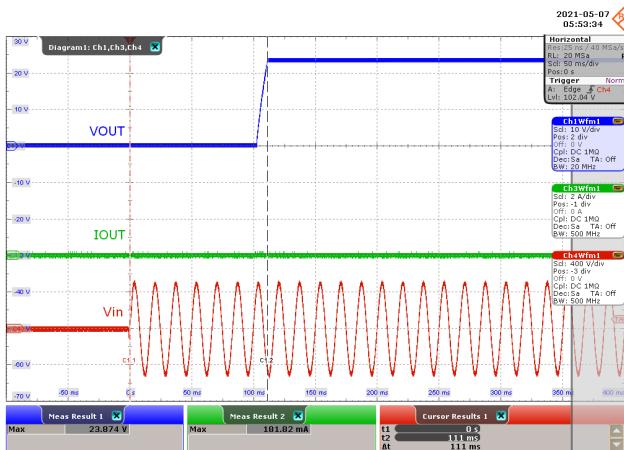
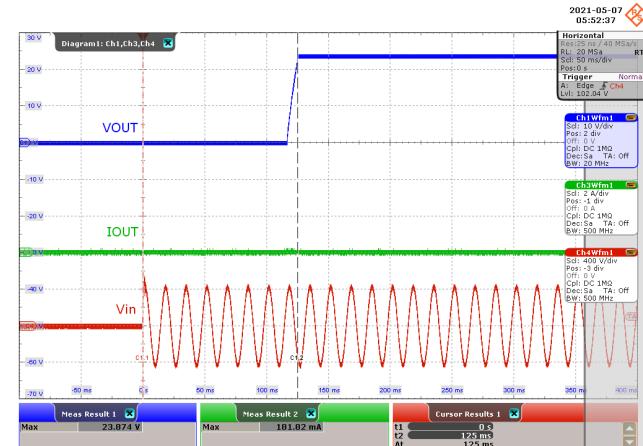
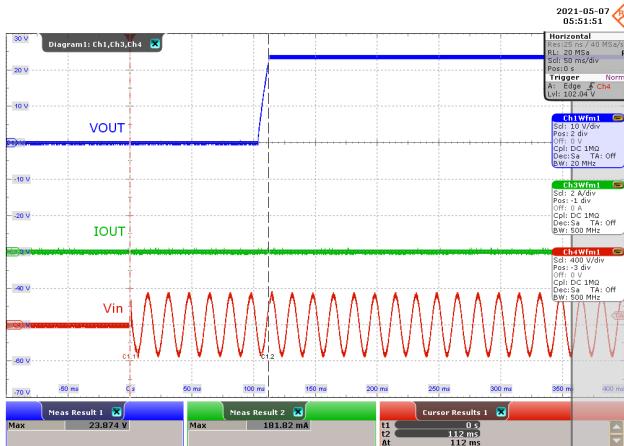
**Figure 32 – 90 VAC 60 Hz.**CH1: V_{OUT}, 10 V / div., 50 ms / div.CH3: I_{OUT}, 2 A / div., 50 ms / div.CH4: V_{IN}, 400 V / div., 50 ms / div.

On-Time Delay = 150 ms.

**Figure 33 – 115 VAC 60 Hz.**CH1: V_{OUT}, 10 V / div., 50 ms / div.CH3: I_{OUT}, 2 A / div., 50 ms / div.CH4: V_{IN}, 400 V / div., 50 ms / div.

On-Time Delay = 186 ms.





11.2.2 CR Mode

11.2.2.1 100% Load

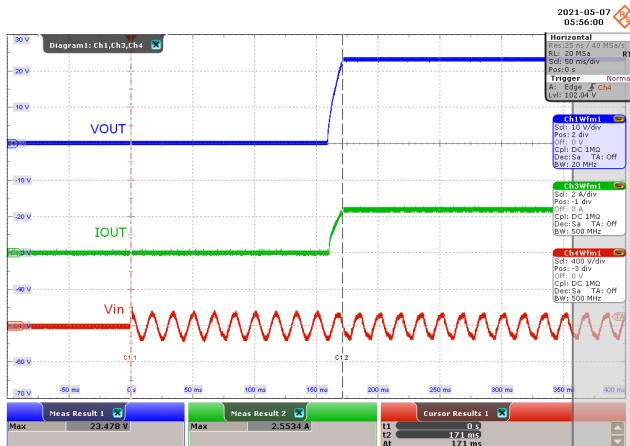


Figure 38 – 90 VAC 60 Hz.

CH1: V_{OUT}, 10 V / div., 50 ms / div.
 CH3: I_{OUT}, 2 A / div., 50 ms / div.
 CH4: V_{IN}, 400 V / div., 50 ms / div.
 On-Time Delay = 171 ms.

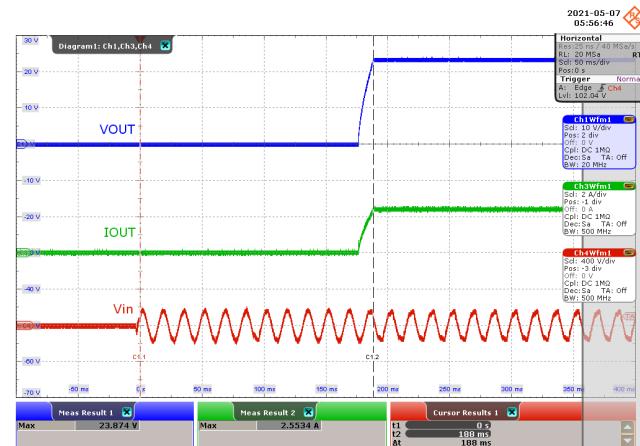


Figure 39 – 115 VAC 60 Hz.

CH1: V_{OUT}, 10 V / div., 50 ms / div.
 CH3: I_{OUT}, 2 A / div., 50 ms / div.
 CH4: V_{IN}, 400 V / div., 50 ms / div.
 On-Time Delay = 188 ms.

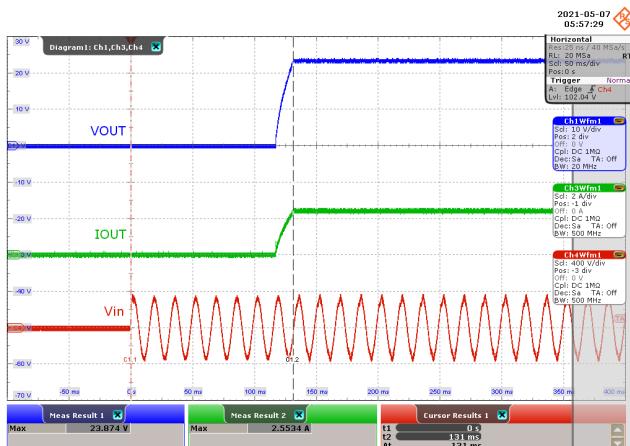


Figure 40 – 230 VAC 60 Hz.

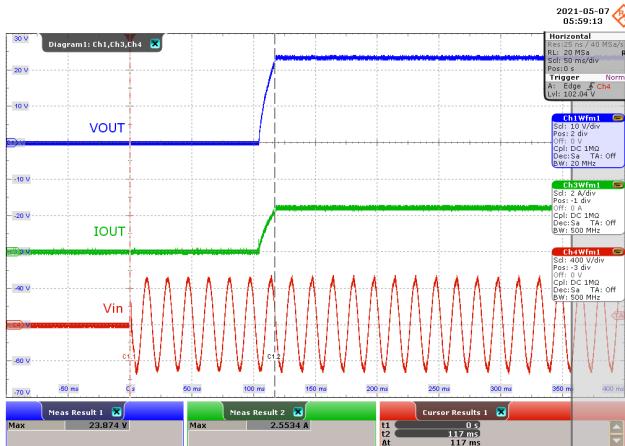
CH1: V_{OUT}, 10 V / div., 50 ms / div.
 CH3: I_{OUT}, 2 A / div., 50 ms / div.
 CH4: V_{IN}, 400 V / div., 50 ms / div.
 On-Time Delay = 131 ms.



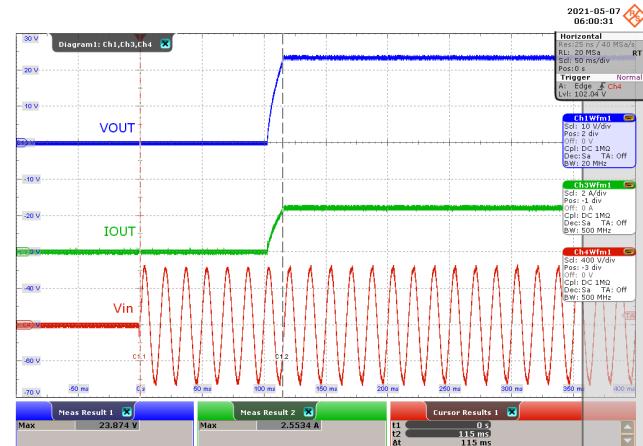
Figure 41 – 300 VAC 60 Hz.

CH1: V_{OUT}, 10 V / div., 50 ms / div.
 CH3: I_{OUT}, 2 A / div., 50 ms / div.
 CH4: V_{IN}, 400 V / div., 50 ms / div.
 On-Time Delay = 131 ms.



**Figure 42 – 350 VAC 60 Hz.**CH1: V_{OUT}, 10 V / div., 50 ms / div.CH3: I_{OUT}, 2 A / div., 50 ms / div.CH4: V_{IN}, 400 V / div., 50 ms / div.

On-Time Delay = 117 ms.

**Figure 43 – 440 VAC 60 Hz.**CH1: V_{OUT}, 10 V / div., 50 ms / div.CH3: I_{OUT}, 2 A / div., 50 ms / div.CH4: V_{IN}, 400 V / div., 50 ms / div.

On-Time Delay = 115 ms.



11.3 MinE-CAP Waveforms

11.3.1 MinE-CAP Normal Operation at 100% Load

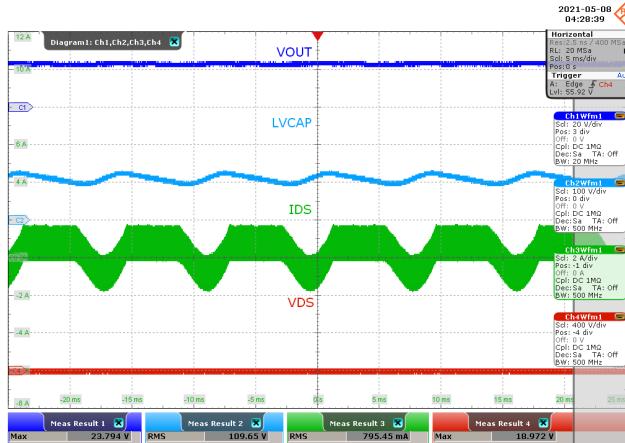


Figure 44 – 90 VAC 60 Hz.

CH1: V_{OUT}, 20 V / div., 5 ms / div.
 CH2: V_{LV_CAP}, 100 V / div., 5 ms / div.
 CH3: I_{DS}, 2 A / div., 5 ms / div.
 CH4: V_{DS}, 400 V / div., 5 ms / div.
 $V_{LV_CAP} = 109.65 \text{ V}_{RMS}$.

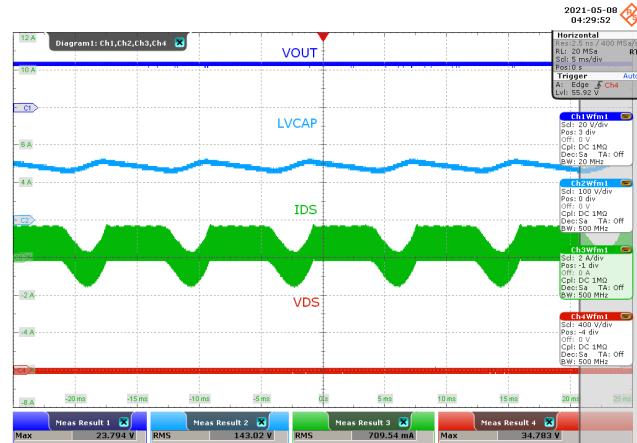


Figure 45 – 115 VAC 60 Hz.

CH1: V_{OUT}, 20 V / div., 5 ms / div.
 CH2: V_{LV_CAP}, 100 V / div., 5 ms / div.
 CH3: I_{DS}, 2 A / div., 5 ms / div.
 CH4: V_{DS}, 400 V / div., 5 ms / div.
 $V_{LV_CAP} = 143.02 \text{ V}_{RMS}$.

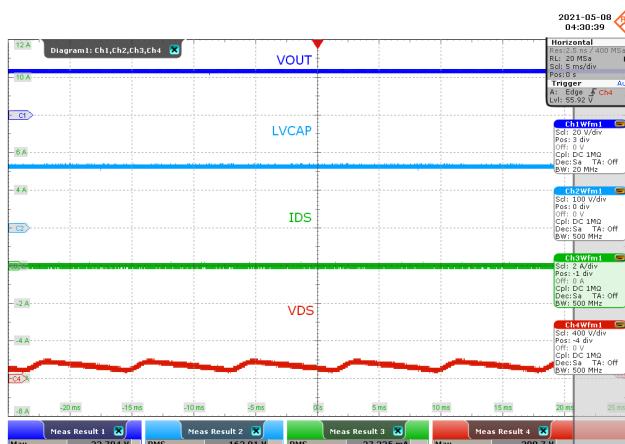


Figure 46 – 230 VAC 60 Hz.

CH1: V_{OUT}, 20 V / div., 5 ms / div.
 CH2: V_{LV_CAP}, 100 V / div., 5 ms / div.
 CH3: I_{DS}, 2 A / div., 5 ms / div.
 CH4: V_{DS}, 400 V / div., 5 ms / div.
 $V_{LV_CAP} = 162.91 \text{ V}_{RMS}$.

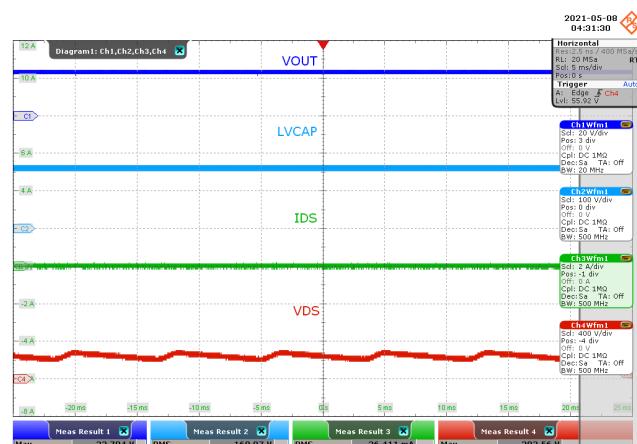


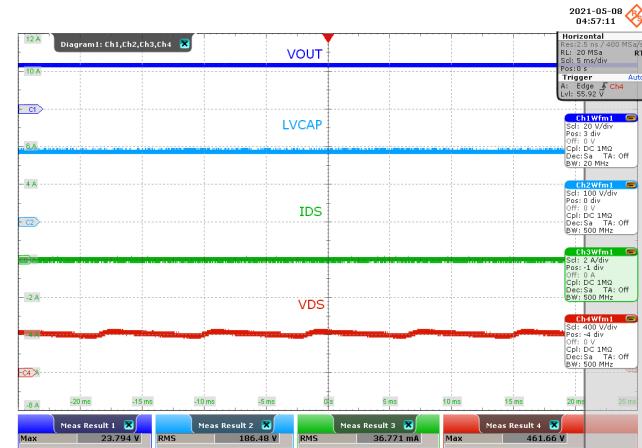
Figure 47 – 300 VAC 60 Hz.

CH1: V_{OUT}, 20 V / div., 5 ms / div.
 CH2: V_{LV_CAP}, 100 V / div., 5 ms / div.
 CH3: I_{DS}, 2 A / div., 5 ms / div.
 CH4: V_{DS}, 400 V / div., 5 ms / div.
 $V_{LV_CAP} = 160.87 \text{ V}_{RMS}$.



**Figure 48 – 350 VAC 60 Hz.**

CH1: V_{OUT}, 20 V / div., 5 ms / div.
 CH2: V_{LV_CAP}, 100 V / div., 5 ms / div.
 CH3: I_{DS}, 2 A / div., 5 ms / div.
 CH4: V_{DS}, 400 V / div., 5 ms / div.
 V_{LV_CAP} = 187.53 V_{RMS}.

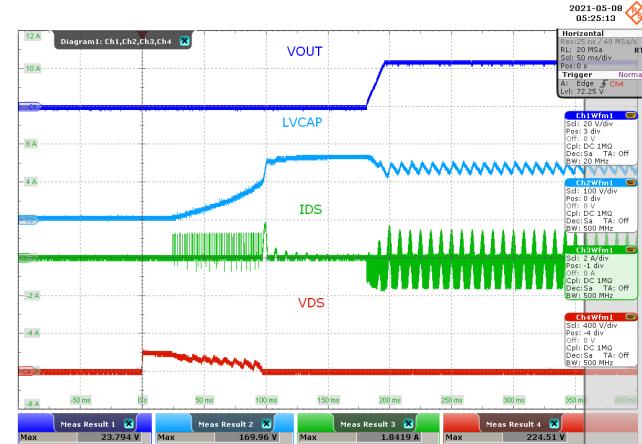
**Figure 49 – 440 VAC 60 Hz.**

CH1: V_{OUT}, 20 V / div., 5 ms / div.
 CH2: V_{LV_CAP}, 100 V / div., 5 ms / div.
 CH3: I_{DS}, 2 A / div., 5 ms / div.
 CH4: V_{DS}, 400 V / div., 5 ms / div.
 V_{LV_CAP} = 186.48 V_{RMS}.

11.3.2 MinE-CAP Start-up at 100% Load

**Figure 50 – 90 VAC 60 Hz.**

CH1: V_{OUT}, 20 V / div., 50 ms / div.
 CH2: V_{LV_CAP}, 100 V / div., 50 ms / div.
 CH3: I_{DS}, 2 A / div., 50 ms / div.
 CH4: V_{DS}, 400 V / div., 50 ms / div.
 V_{LV_CAP} = 142.29 V_{MAX}.

**Figure 51 – 115 VAC 60 H.**

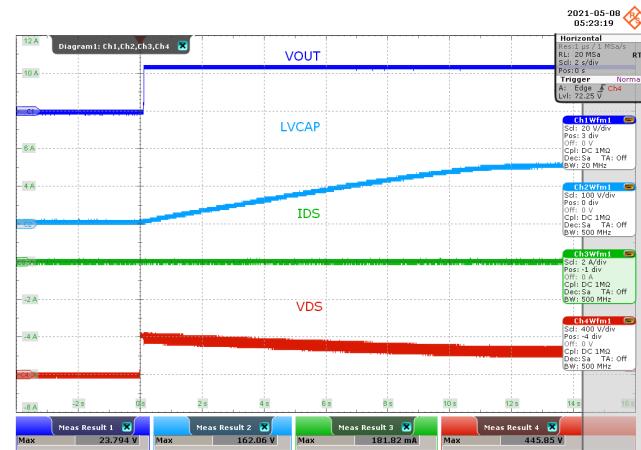
CH1: V_{OUT}, 20 V / div., 50 ms / div.
 CH2: V_{LV_CAP}, 100 V / div., 50 ms / div.
 CH3: I_{DS}, 2 A / div., 50 ms / div.
 CH4: V_{DS}, 400 V / div., 50 ms / div.
 V_{LV_CAP} = 169.96 V_{MAX}.



**Figure 52 – 230 VAC 60 Hz.**

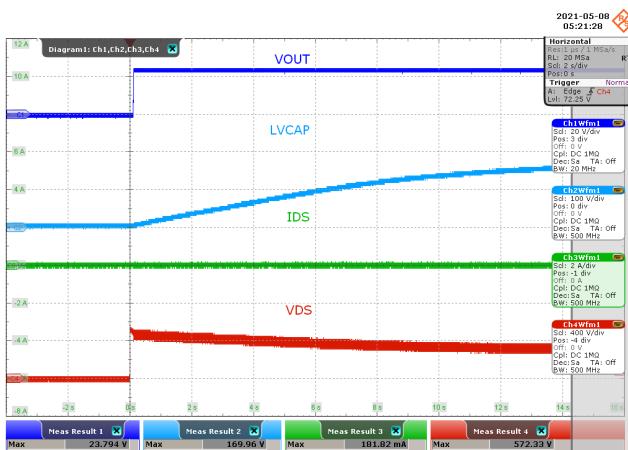
CH1: V_{OUT}, 20 V / div., 2 s / div.
 CH2: V_{LV_CAP}, 100 V / div., 2 s / div.
 CH3: I_{DS}, 2 A / div., 2 s / div.
 CH4: V_{DS}, 400 V / div., 2 s / div.

$$V_{LV_CAP} = 166.01 \text{ V}_{MAX}$$

**Figure 53 – 300 VAC 60 Hz.**

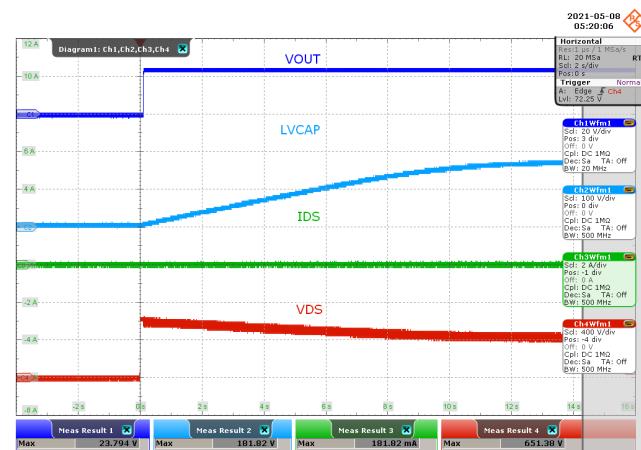
CH1: V_{OUT}, 20 V / div., 2 s / div.
 CH2: V_{LV_CAP}, 100 V / div., 2 s / div.
 CH3: I_{DS}, 2 A / div., 2 s / div.
 CH4: V_{DS}, 400 V / div., 2 s / div.

$$V_{LV_CAP} = 162.06 \text{ V}_{MAX}$$

**Figure 54 – 350 VAC 60 Hz.**

CH1: V_{OUT}, 20 V / div., 2 s / div.
 CH2: V_{LV_CAP}, 100 V / div., 2 s / div.
 CH3: I_{DS}, 2 A / div., 2 s / div.
 CH4: V_{DS}, 400 V / div., 2 s / div.

$$V_{LV_CAP} = 169.96 \text{ V}_{MAX}$$

**Figure 55 – 440 VAC 60 Hz.**

CH1: V_{OUT}, 20 V / div., 2 s / div.
 CH2: V_{LV_CAP}, 100 V / div., 2 s / div.
 CH3: I_{DS}, 2 A / div., 2 s / div.
 CH4: V_{DS}, 400 V / div., 2 s / div.

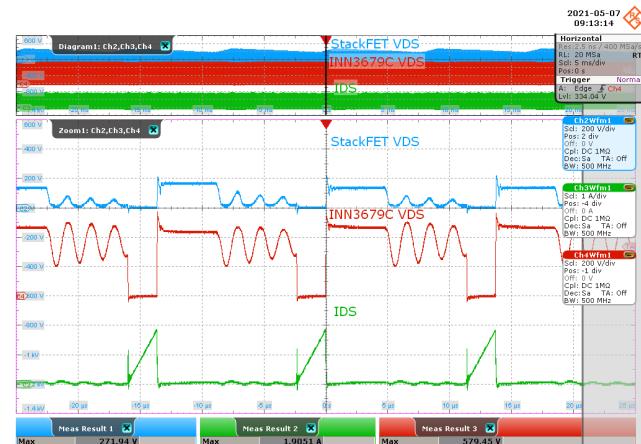
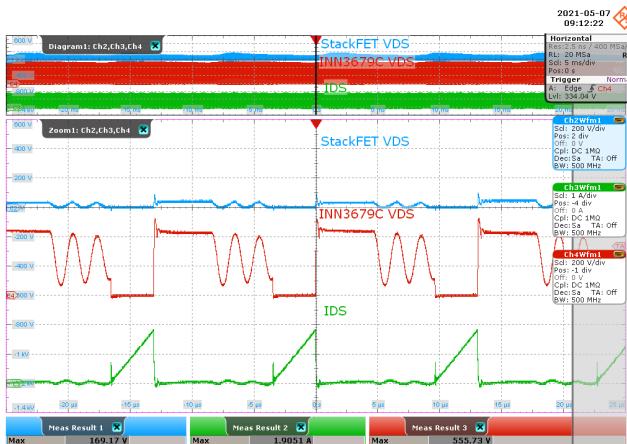
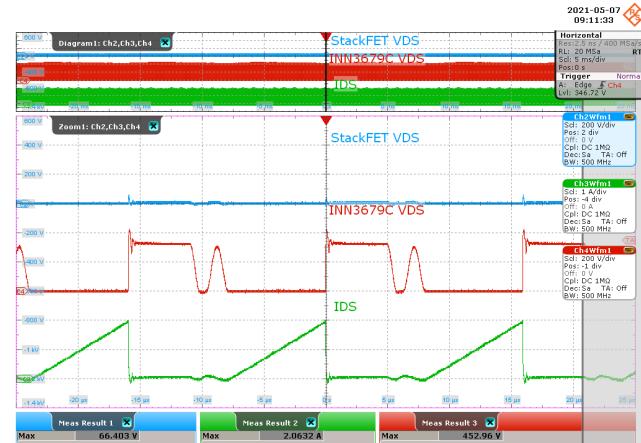
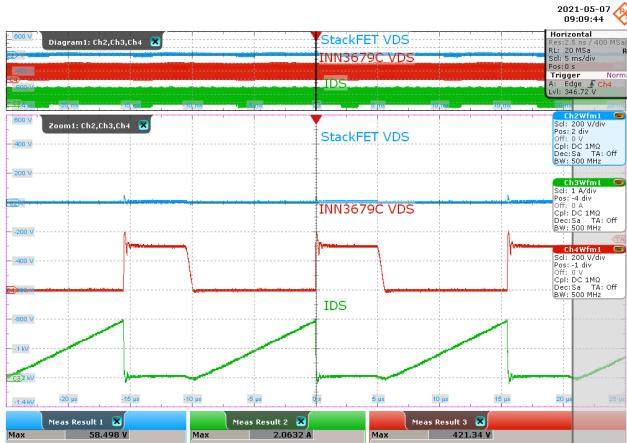
$$V_{LV_CAP} = 181.82 \text{ V}_{MAX}$$

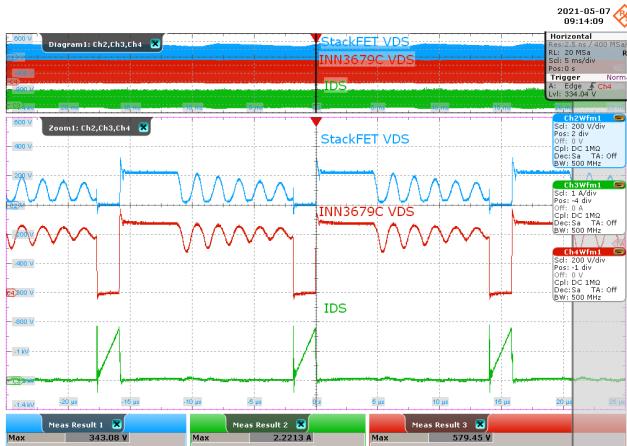


11.4 Switching Waveforms

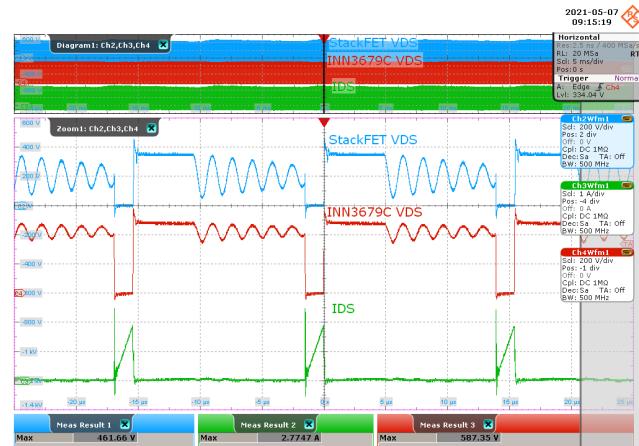
11.4.1 Primary MOSFET and StackFET Drain-Source Voltage and Current at Normal Operation

11.4.1.1 100% Load



**Figure 60 – 350 VAC 60 Hz.**

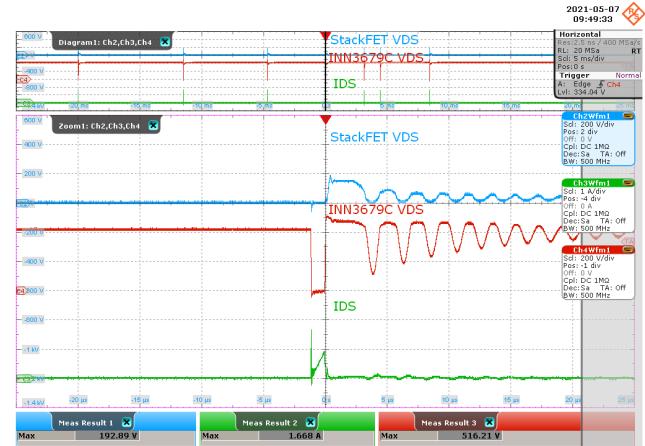
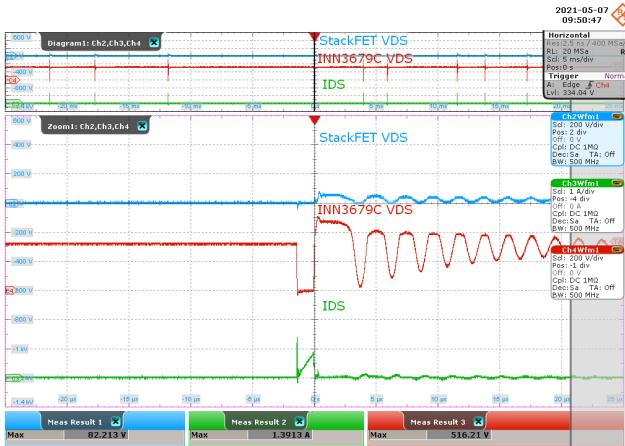
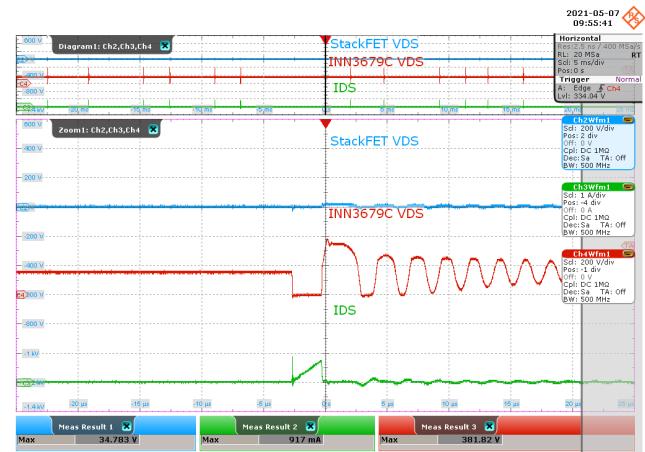
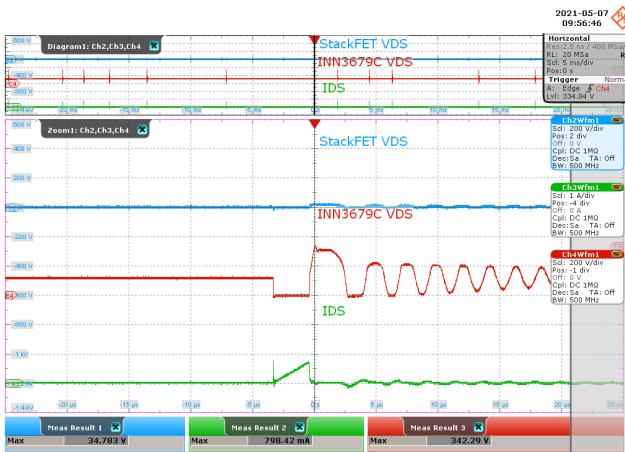
CH2: StackFET V_{DS} , 200 V / div., 5 ms / div.
 CH3: I_{DS} , 1 A / div., 5 ms / div.
 CH4: INN3679C V_{DS} , 200 V / div., 5 ms / div.
 INN3679C $V_{DS(MAX)}$ = 579.45 V.
 $I_{DS(MAX)}$ = 2.22 A.
 StackFET $V_{DS(MAX)}$ = 343.08 V.

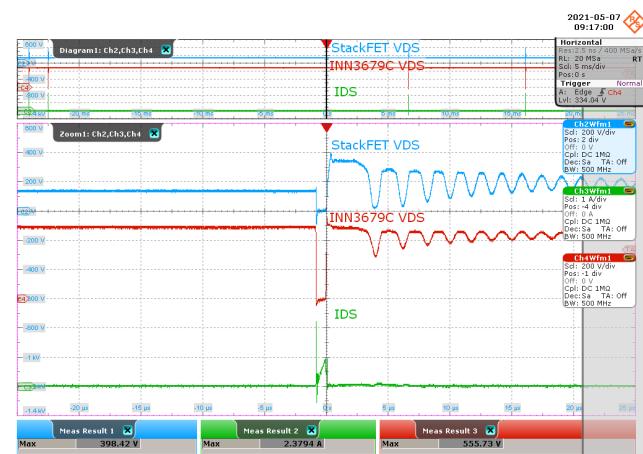
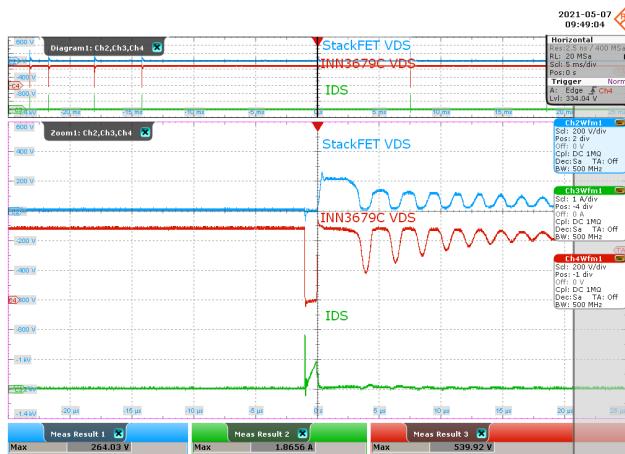
**Figure 61 – 440 VAC 60 Hz.**

CH2: StackFET V_{DS} , 200 V / div., 5 ms / div.
 CH3: I_{DS} , 1 A / div., 5 ms / div.
 CH4: INN3679C V_{DS} , 200 V / div., 5 ms / div.
 INN3679C $V_{DS(MAX)}$ = 587.35 V.
 $I_{DS(MAX)}$ = 2.77 A.
 StackFET $V_{DS(MAX)}$ = 461.66 V.



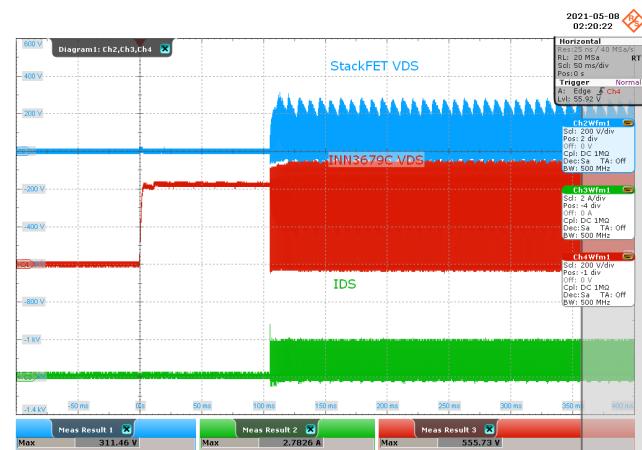
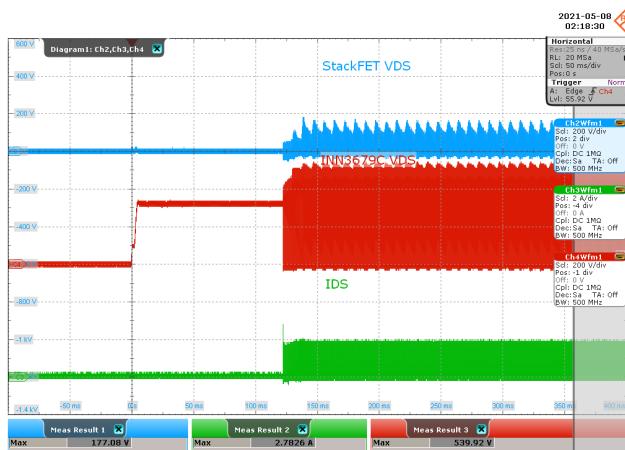
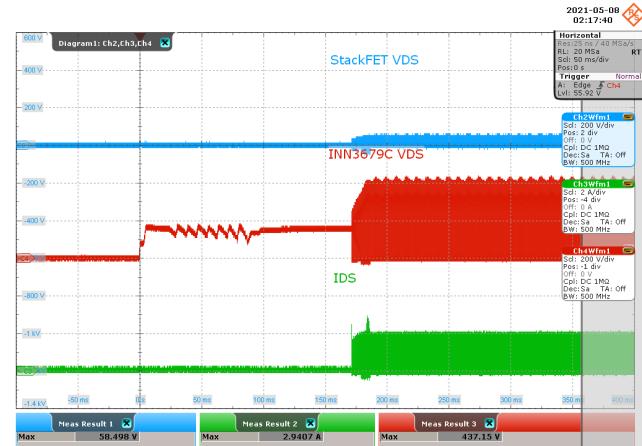
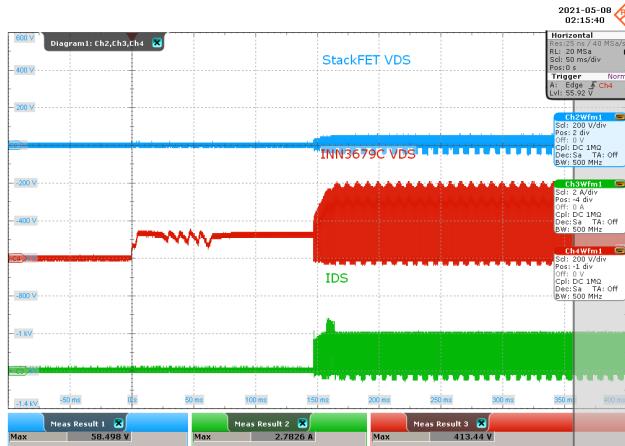
11.4.1.2 0% Load

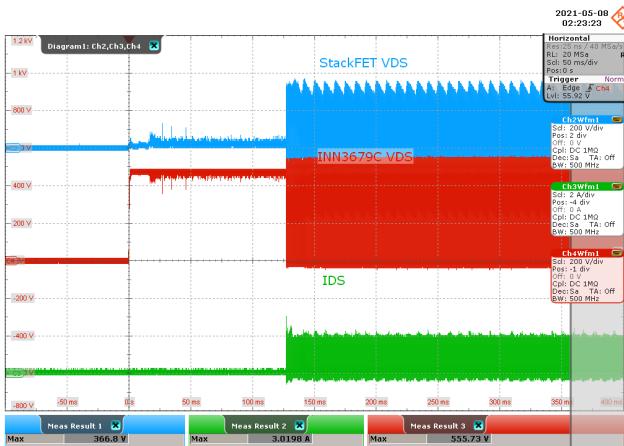




11.4.2 Primary MOSFET Drain-Source Voltage and Current at Start-up Operation

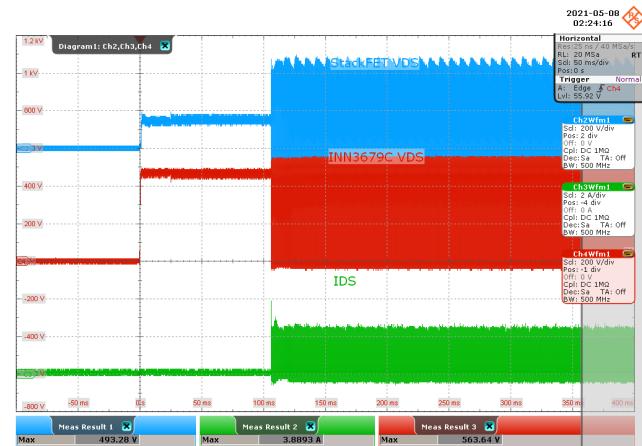
11.4.2.1 100% Load



**Figure 72 – 350 VAC 60 Hz.**

CH2: StackFET V_{DS} , 200 V / div., 50 ms / div.
CH3: I_{DS} , 2 A / div., 50 ms / div.

CH4: INN3679C V_{DS} , 200 V / div., 50 ms / div.
INN3679C $V_{DS(MAX)}$ = 555.73 V.
 $I_{DS(MAX)}$ = 3.02 A.
StackFET $V_{DS(MAX)}$ = 366.80 V.

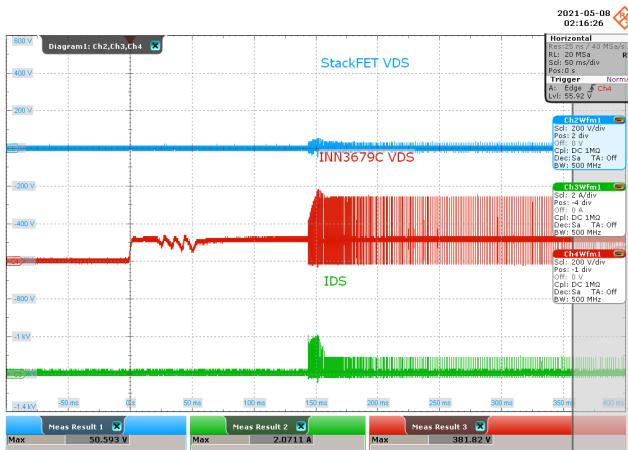
**Figure 73 – 440 VAC 60 Hz.**

CH2: StackFET V_{DS} , 200 V / div., 50 ms / div.
CH3: I_{DS} , 2 A / div., 50 ms / div.

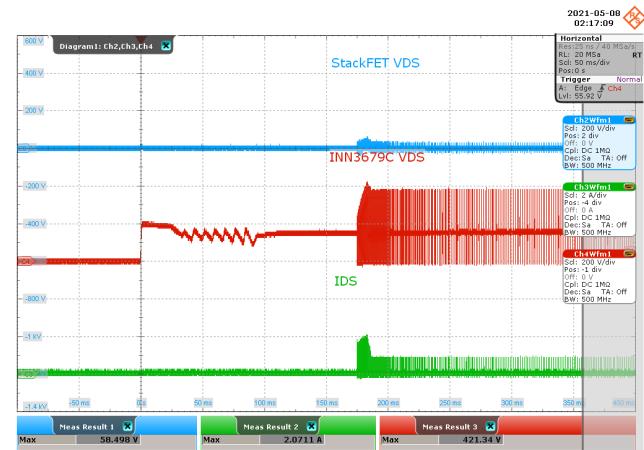
CH4: INN3679C V_{DS} , 200 V / div., 50 ms / div.
INN3679C $V_{DS(MAX)}$ = 563.64 V.
 $I_{DS(MAX)}$ = 3.89 A.
StackFET $V_{DS(MAX)}$ = 493.28 V.



11.4.2.2 0% Load

**Figure 74 – 90 VAC 60 Hz.**

CH2: StackFET V_{DS} , 200 V / div., 50 ms / div.
 CH3: I_{DS} , 2 A / div., 50 ms / div.
 CH4: INN3679C V_{DS} , 200 V / div., 50 ms / div.
 INN3679C $V_{DS(\text{MAX})} = 381.82 \text{ V}$.
 $I_{DS(\text{MAX})} = 2.07 \text{ A}$.
 StackFET $V_{DS(\text{MAX})} = 50.59 \text{ V}$.

**Figure 75 – 115 VAC 60 Hz.**

CH2: StackFET V_{DS} , 200 V / div., 50 ms / div.
 CH3: I_{DS} , 2 A / div., 50 ms / div.
 CH4: INN3679C V_{DS} , 200 V / div., 50 ms / div.
 INN3679C $V_{DS(\text{MAX})} = 421.34 \text{ V}$.
 $I_{DS(\text{MAX})} = 2.07 \text{ A}$.
 StackFET $V_{DS(\text{MAX})} = 58.50 \text{ V}$.

**Figure 76 – 230 VAC 60 Hz.**

CH2: StackFET V_{DS} , 200 V / div., 50 ms / div.
 CH3: I_{DS} , 2 A / div., 50 ms / div.
 CH4: INN3679C V_{DS} , 200 V / div., 50 ms / div.
 INN3679C $V_{DS(\text{MAX})} = 516.21 \text{ V}$.
 $I_{DS(\text{MAX})} = 2.31 \text{ A}$.
 StackFET $V_{DS(\text{MAX})} = 137.55 \text{ V}$.

**Figure 77 – 300 VAC 60 Hz.**

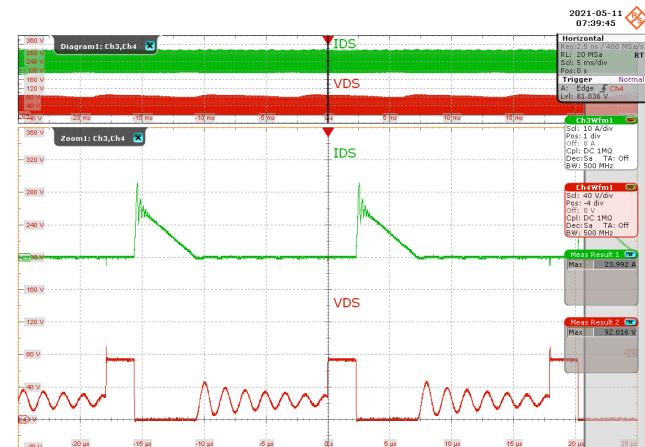
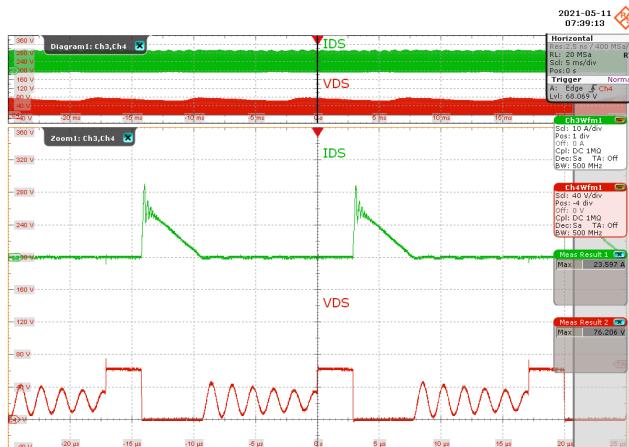
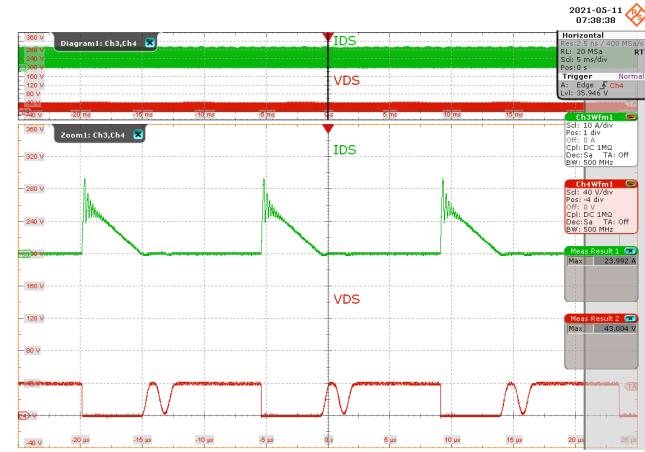
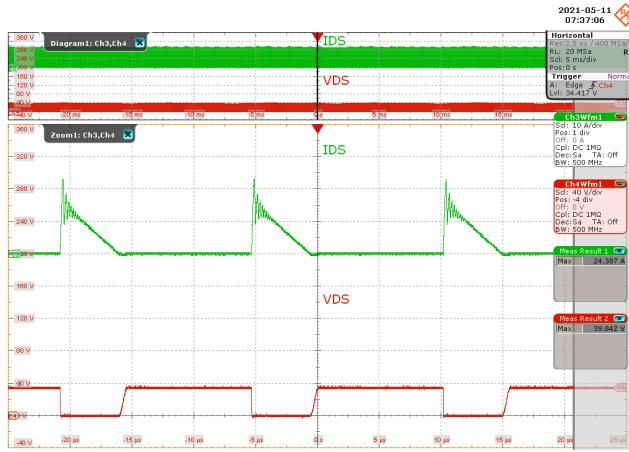
CH2: StackFET V_{DS} , 200 V / div., 50 ms / div.
 CH3: I_{DS} , 2 A / div., 50 ms / div.
 CH4: INN3679C V_{DS} , 200 V / div., 50 ms / div.
 INN3679C $V_{DS(\text{MAX})} = 539.92 \text{ V}$.
 $I_{DS(\text{MAX})} = 2.78 \text{ A}$.
 StackFET $V_{DS(\text{MAX})} = 279.84 \text{ V}$.

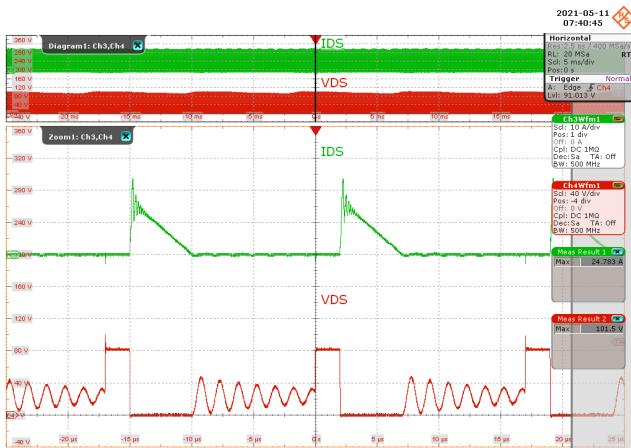




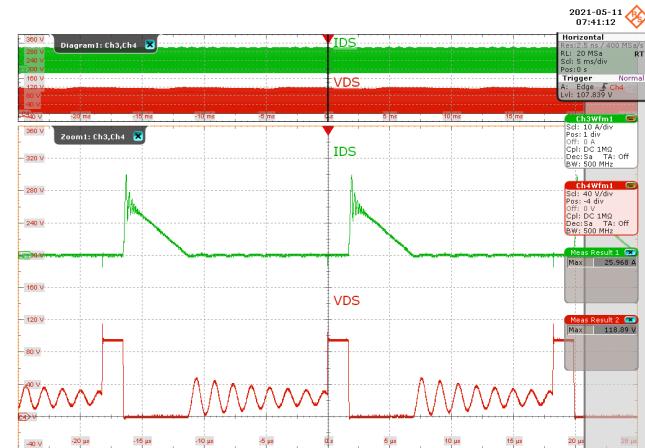
11.4.3 SR FET Voltage and Current at Normal Operation

11.4.3.1 100% Load



**Figure 84 – 350 VAC 60 Hz.**

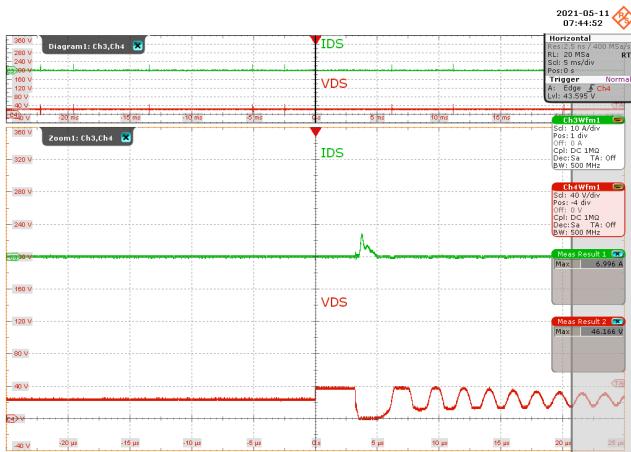
CH3: I_{DS} , 10 A / div., 5 ms / div.
 CH4: V_{DS} , 40 V / div., 5 ms / div.
 Zoom: 5 μ s / div.
 $V_{DS(MAX)} = 101.5$ V, $I_{DS(MAX)} = 24.78$ A.

**Figure 85 – 440 VAC 60 Hz.**

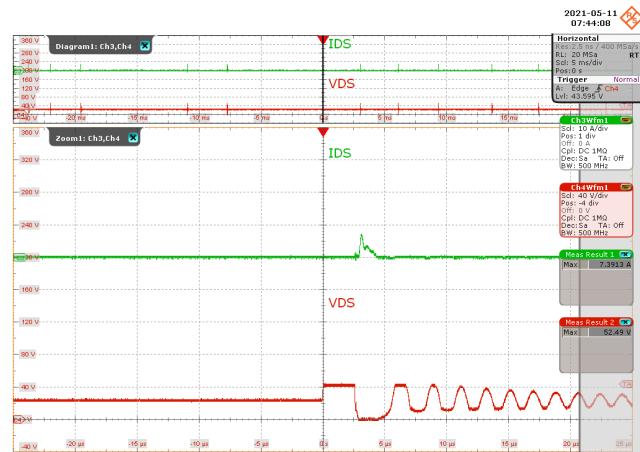
CH3: I_{DS} , 10 A / div., 5 ms / div.
 CH4: V_{DS} , 40 V / div., 5 ms / div.
 Zoom: 5 μ s / div.
 $V_{DS(MAX)} = 118.89$ V, $I_{DS(MAX)} = 25.97$ A.



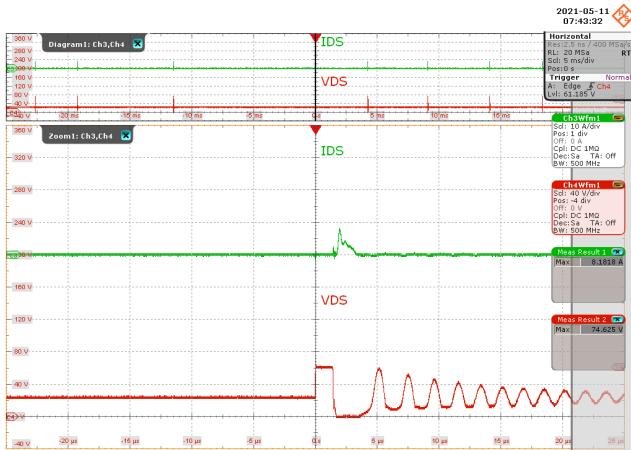
11.4.3.2 0% Load

**Figure 86 – 90 VAC 60 Hz.**

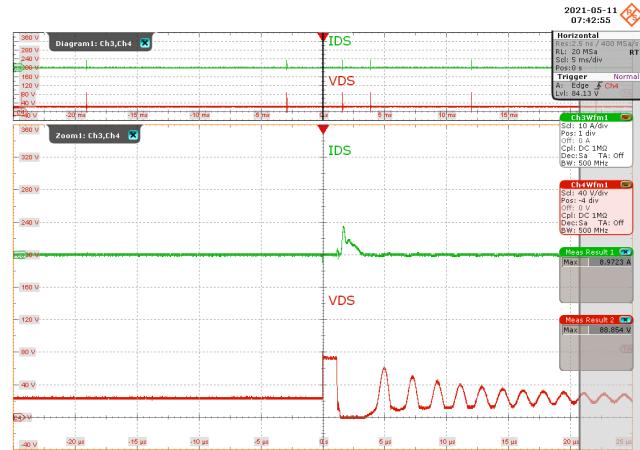
CH3: I_{DS} , 10 A / div., 5 ms / div.
 CH4: V_{DS} , 40 V / div., 5 ms / div.
 Zoom: 5 μs / div.
 $V_{DS(\text{MAX})} = 46.166 \text{ V}$, $I_{DS(\text{MAX})} = 6.996 \text{ A}$.

**Figure 87 – 115 VAC 60 Hz.**

CH3: I_{DS} , 10 A / div., 5 ms / div.
 CH4: V_{DS} , 40 V / div., 5 ms / div.
 Zoom: 5 μs / div.
 $V_{DS(\text{MAX})} = 52.49 \text{ V}$, $I_{DS(\text{MAX})} = 7.39 \text{ A}$.

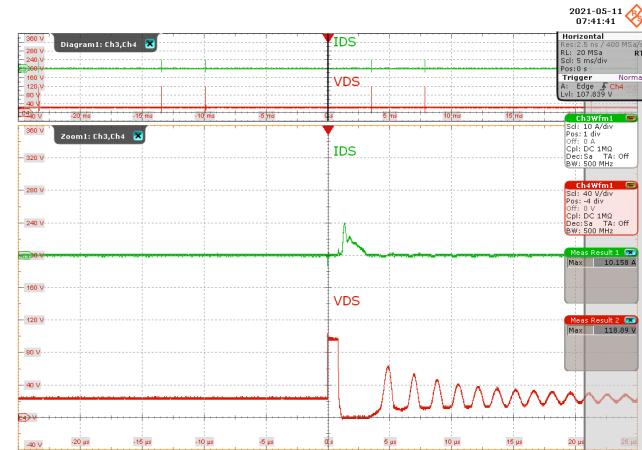
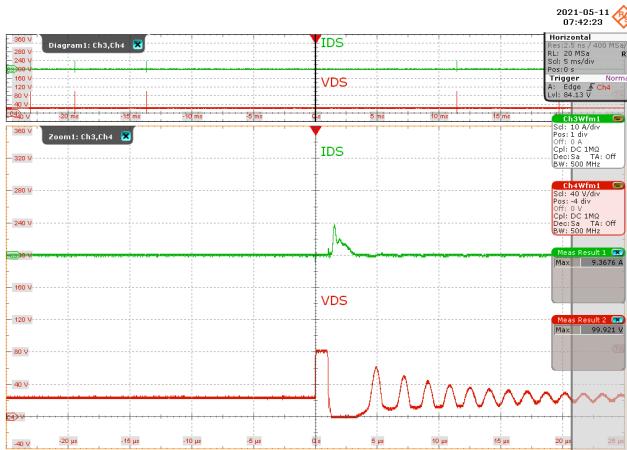
**Figure 88 – 230 VAC 60 Hz.**

CH3: I_{DS} , 10 A / div., 5 ms / div.
 CH4: V_{DS} , 40 V / div., 5 ms / div.
 Zoom: 5 μs / div.
 $V_{DS(\text{MAX})} = 74.63 \text{ V}$, $I_{DS(\text{MAX})} = 8.18 \text{ A}$.

**Figure 89 – 300 VAC 60 Hz.**

CH3: I_{DS} , 10 A / div., 5 ms / div.
 CH4: V_{DS} , 40 V / div., 5 ms / div.
 Zoom: 5 μs / div.
 $V_{DS(\text{MAX})} = 88.85 \text{ V}$, $I_{DS(\text{MAX})} = 8.97 \text{ A}$.





11.4.4 SR FET Voltage and Current at Start-up Operation

11.4.4.1 100% Load



Figure 92 – 90 VAC 60 Hz.

CH3: I_{DS} , 10 A / div., 5 ms / div.
CH4: V_{DS} , 40 V / div., 5 ms / div.
Zoom: 50 μ s / div.
 $V_{DS(MAX)} = 87.27$ V, $I_{DS(MAX)} = 24.39$ A.

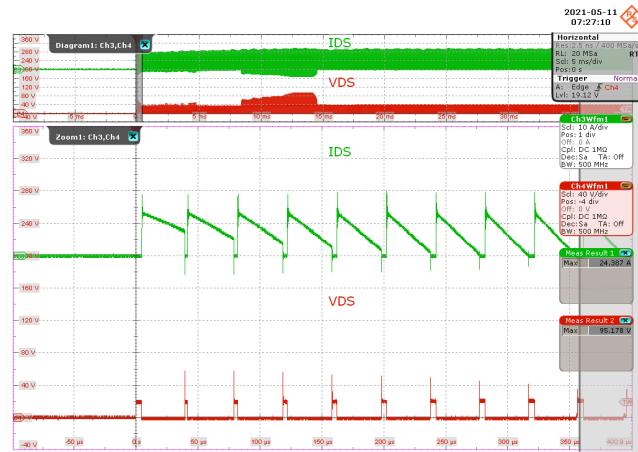


Figure 93 – 115 VAC 60 Hz.

CH3: I_{DS} , 10 A / div., 5 ms / div.
CH4: V_{DS} , 40 V / div., 5 ms / div.
Zoom: 50 μ s / div.
 $V_{DS(MAX)} = 95.18$ V, $I_{DS(MAX)} = 24.39$ A.



Figure 94 – 230 VAC 60 Hz.

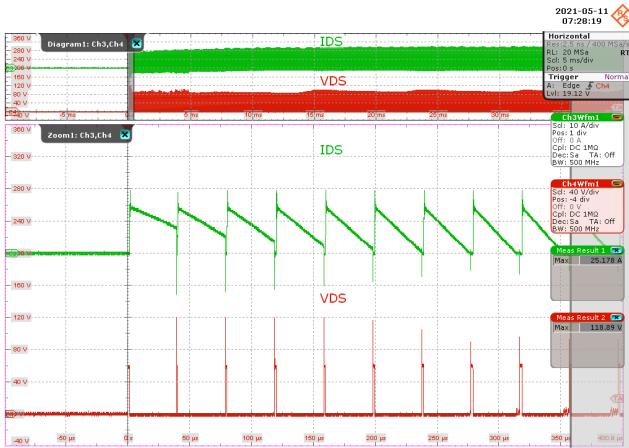
CH3: I_{DS} , 10 A / div., 5 ms / div.
CH4: V_{DS} , 40 V / div., 5 ms / div.
Zoom: 50 μ s / div.
 $V_{DS(MAX)} = 104.66$ V, $I_{DS(MAX)} = 21.62$ A.



Figure 95 – 300 VAC 60 Hz.

CH3: I_{DS} , 10 A / div., 5 ms / div.
CH4: V_{DS} , 40 V / div., 5 ms / div.
Zoom: 50 μ s / div.
 $V_{DS(MAX)} = 118.89$ V, $I_{DS(MAX)} = 22.41$ A.



**Figure 96 – 350 VAC 60 Hz.**

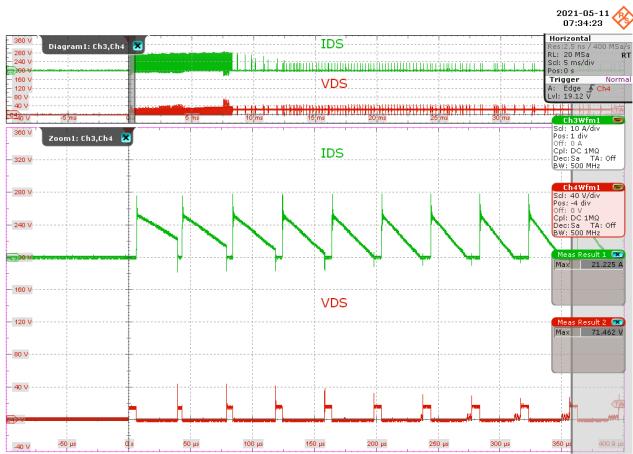
CH3: I_{DS} , 10 A / div., 5 ms / div.
 CH4: V_{DS} , 40 V / div., 5 ms / div.
 Zoom: 50 μ s / div.
 $V_{DS(MAX)} = 118.89$ V, $I_{DS(MAX)} = 25.18$ A.

**Figure 97 – 440 VAC 60 Hz.**

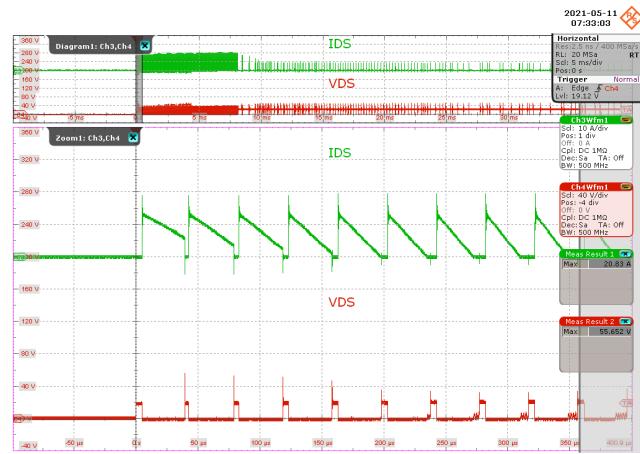
CH3: I_{DS} , 10 A / div., 5 ms / div.
 CH4: V_{DS} , 40 V / div., 5 ms / div.
 Zoom: 50 μ s / div.
 $V_{DS(MAX)} = 118.89$ V, $I_{DS(MAX)} = 25.97$ A.



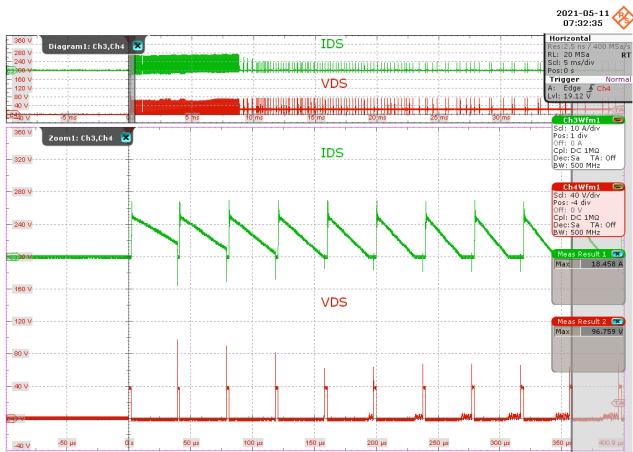
11.4.4.2 0% Load

**Figure 98 – 90 VAC 60 Hz.**

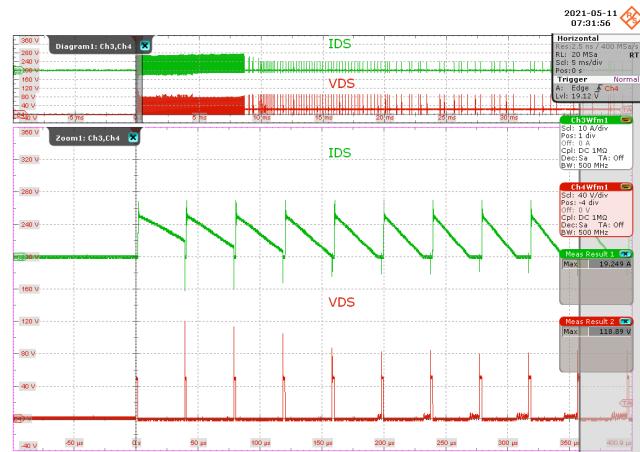
CH3: I_{DS} , 10 A / div., 5 ms / div.
 CH4: V_{DS} , 40 V / div., 5 ms / div.
 Zoom: 50 μ s / div.
 $V_{DS(MAX)} = 71.46$ V, $I_{DS(MAX)} = 21.23$ A.

**Figure 99 – 115 VAC 60 Hz.**

CH3: I_{DS} , 10 A / div., 5 ms / div.
 CH4: V_{DS} , 40 V / div., 5 ms / div.
 Zoom: 50 μ s / div.
 $V_{DS(MAX)} = 55.65$ V, $I_{DS(MAX)} = 20.83$ A.

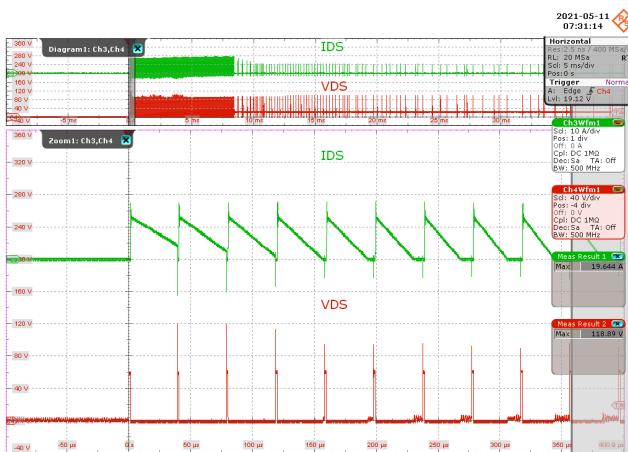
**Figure 100 – 230 VAC 60 Hz.**

CH3: I_{DS} , 10 A / div., 5 ms / div.
 CH4: V_{DS} , 40 V / div., 5 ms / div.
 Zoom: 50 μ s / div.
 $V_{DS(MAX)} = 96.76$ V, $I_{DS(MAX)} = 18.46$ A.

**Figure 101 – 300 VAC 60 Hz.**

CH3: I_{DS} , 10 A / div., 5 ms / div.
 CH4: V_{DS} , 40 V / div., 5 ms / div.
 Zoom: 50 μ s / div.
 $V_{DS(MAX)} = 118.89$ V, $I_{DS(MAX)} = 19.25$ A.



**Figure 102 – 350 VAC 60 Hz.**

CH3: I_{DS} , 10 A / div., 5 ms / div.
 CH4: V_{DS} , 40 V / div., 5 ms / div.
 Zoom: 50 μ s / div.
 $V_{DS(MAX)} = 118.89 \text{ V}$, $I_{DS(MAX)} = 19.64 \text{ A}$.

**Figure 103 – 440 VAC 60 Hz.**

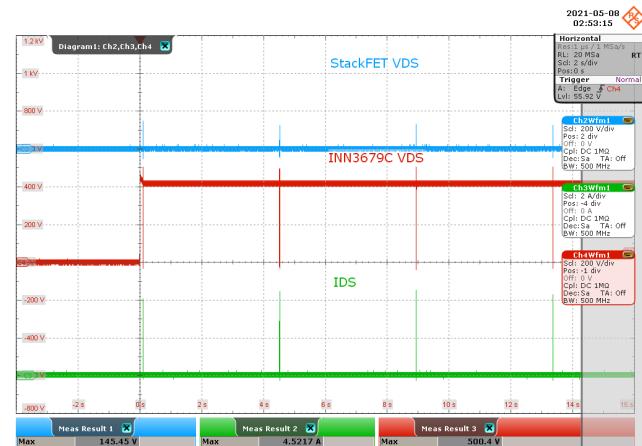
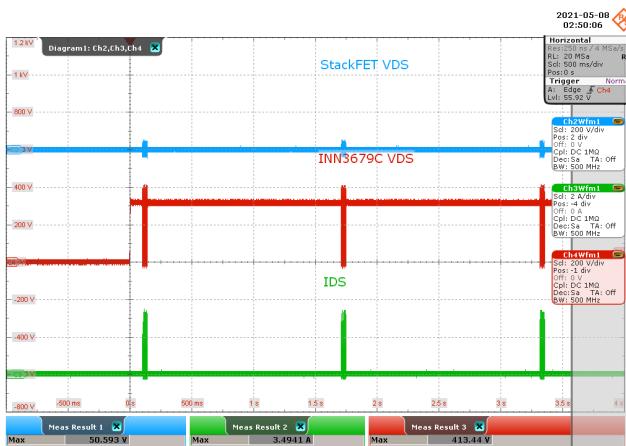
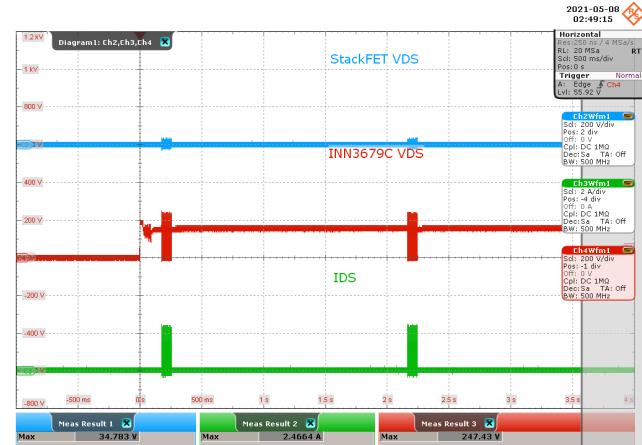
CH3: I_{DS} , 10 A / div., 5 ms / div.
 CH4: V_{DS} , 40 V / div., 5 ms / div.
 Zoom: 50 μ s / div.
 $V_{DS(MAX)} = 118.89 \text{ V}$, $I_{DS(MAX)} = 22.02 \text{ A}$.



11.5 Fault Condition

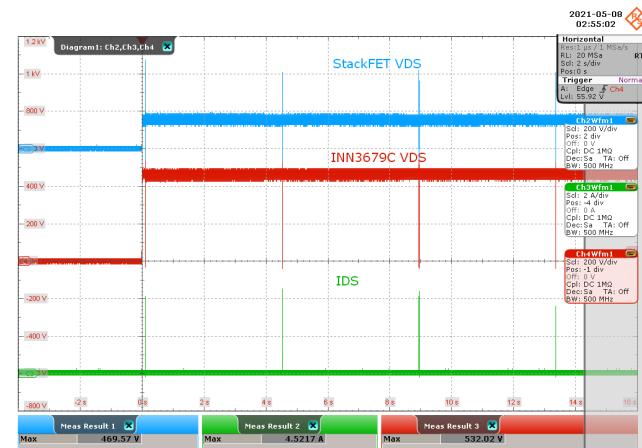
11.5.1 Output Short-Circuit

Test Condition: Short-circuit applied at the end of PCB during start-up



**Figure 108** – 350 VAC 60 Hz.

CH2: StackFET V_{DS} , 200 V / div., 2 s / div.
 CH3: I_{DS} , 2 A / div., 2 s / div.
 CH4: INN3679C V_{DS} , 200 V / div., 2 s / div.
 $INN3679C\ V_{DS(MAX)} = 532.02\ V$.
 $I_{DS(MAX)} = 4.92\ A$.
 $StackFET\ V_{DS(MAX)} = 319.37\ V$.

**Figure 109** – 440 VAC 60 Hz.

CH2: StackFET V_{DS} , 200 V / div., 2 s / div.
 CH3: I_{DS} , 2 A / div., 2 s / div.
 CH4: INN3679C V_{DS} , 200 V / div., 2 s / div.
 $INN3679C\ V_{DS(MAX)} = 532.02\ V$.
 $I_{DS(MAX)} = 4.52\ A$.
 $StackFET\ V_{DS(MAX)} = 469.57\ V$.



11.6 Output Voltage Ripple

11.6.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V X7R ceramic type and one (1) 47 μF / 25 V aluminum electrolytic KZE series from Nippon Chemi-Con. It is recommended to make the capacitor leads as short as possible so as to further reduce the magnitude of spurious signals. The aluminum electrolytic type capacitor is also polarized, so proper polarity across DC outputs must be maintained (see below).

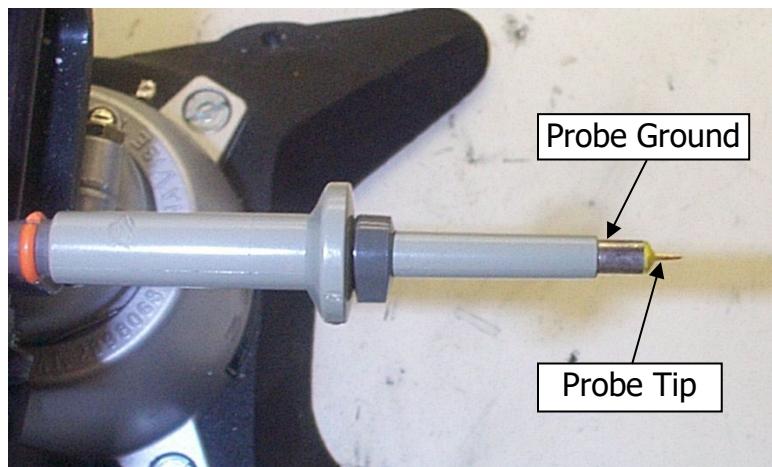


Figure 110 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)



Figure 111 – Probe Master (www.probmast.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

11.6.2 Measurement Results

Note: All ripple measurements were taken at the end of PCB.

11.6.2.1 100% Load Condition

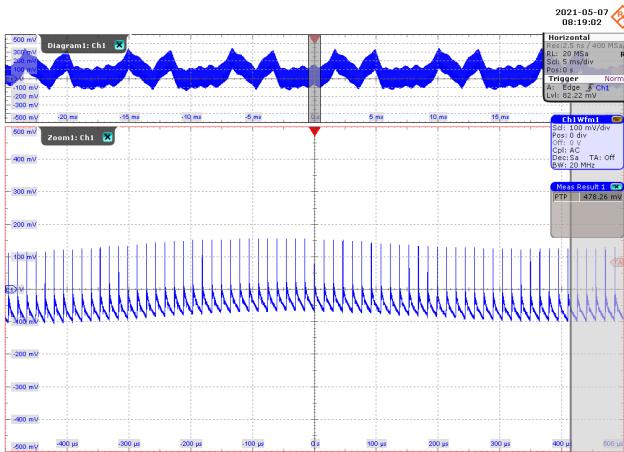


Figure 112 – 90 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 478.26 mV.

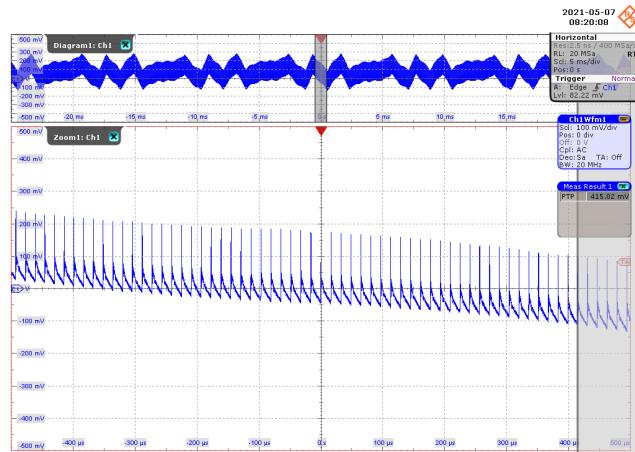


Figure 113 – 115 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 415.02 mV.

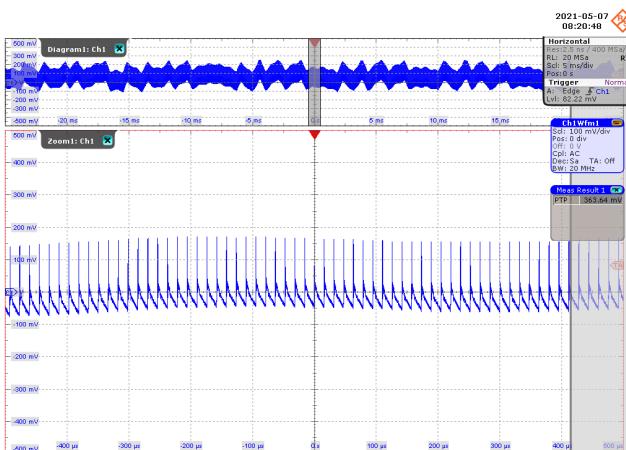


Figure 114 – 230 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 363.64 mV.

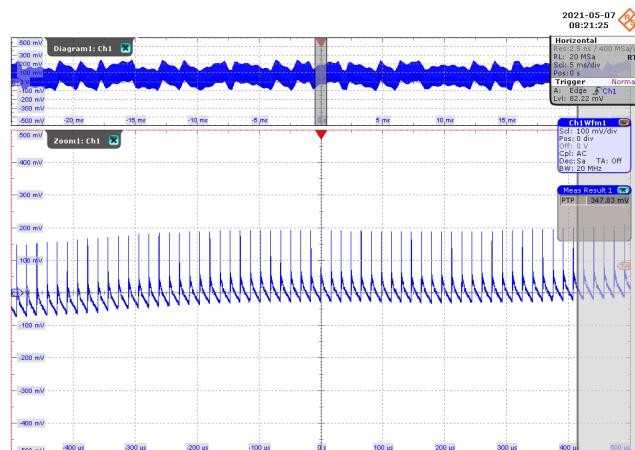


Figure 115 – 300 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 347.83 mV.



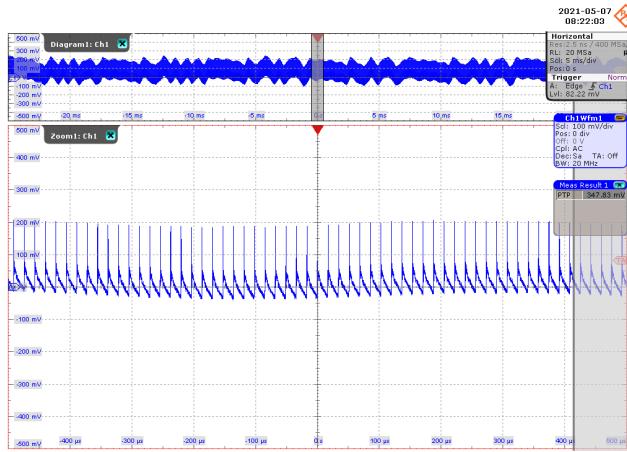


Figure 116 – 350 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 347.83 mV.

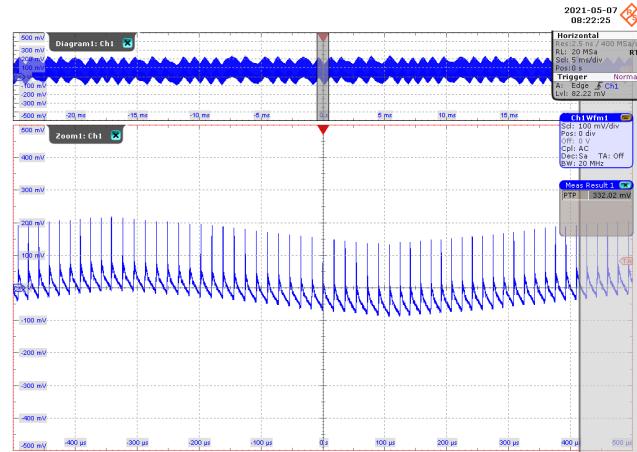


Figure 117 – 440 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 332.02 mV.

11.6.2.2 75% Load Condition

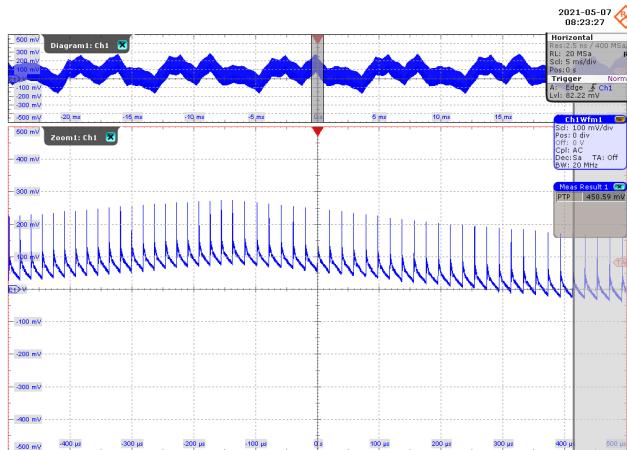


Figure 118 – 90 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 450.59 mV.

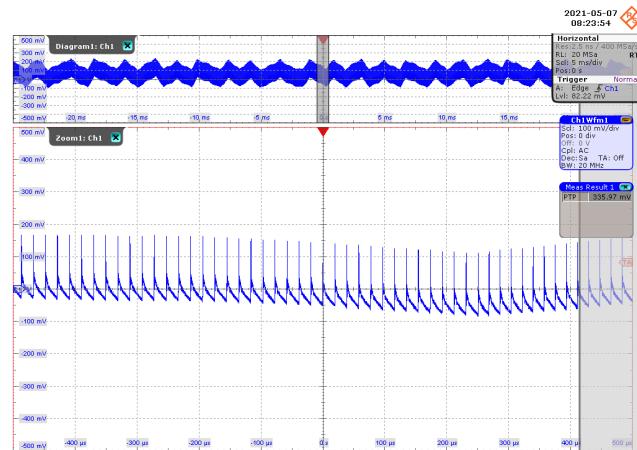


Figure 119 – 115 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 335.97 mV.



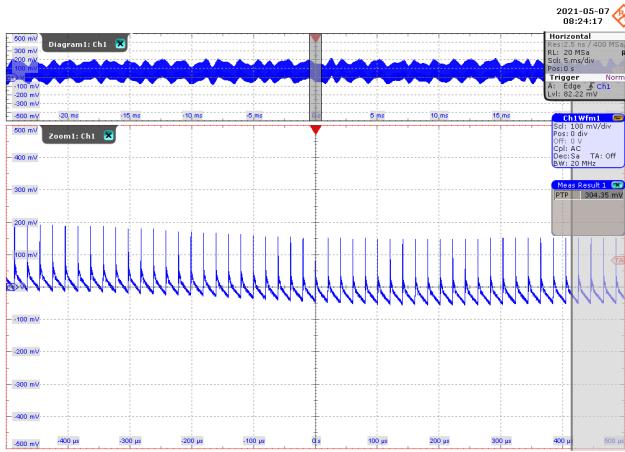


Figure 120 – 230 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 304.35 mV.

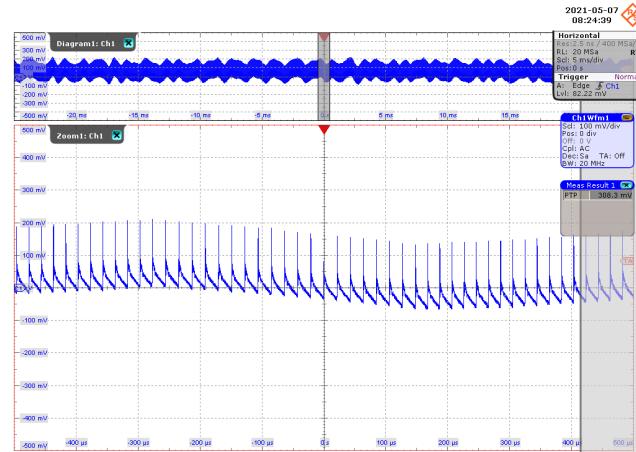


Figure 121 – 300 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 308.30 mV.

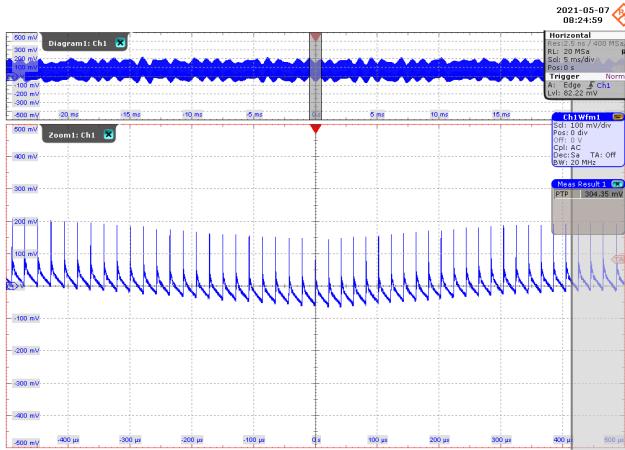


Figure 122 – 350 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 304.35 mV.

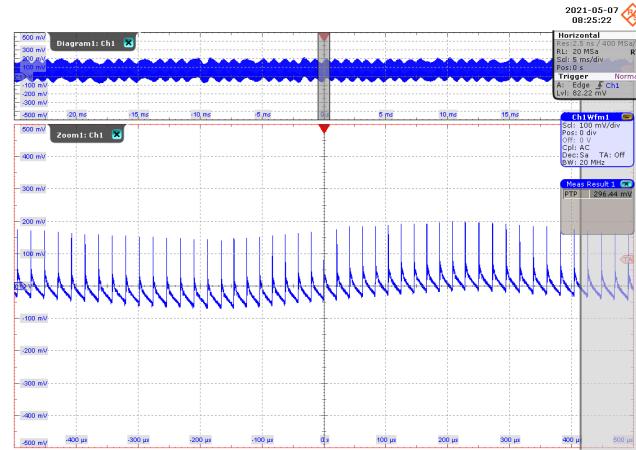


Figure 123 – 440 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 296.44 mV.



11.6.2.3 50% Load Condition

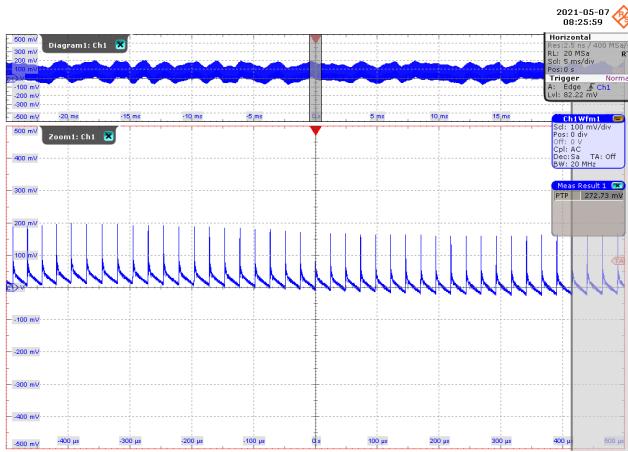


Figure 124 – 90 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
Zoom: 100 μ s / div.
Output Ripple = 272.73 mV.

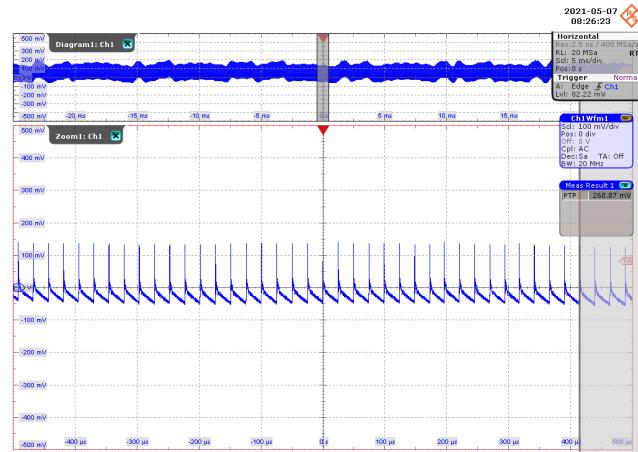


Figure 125 – 115 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
Zoom: 100 μ s / div.
Output Ripple = 260.87 mV.

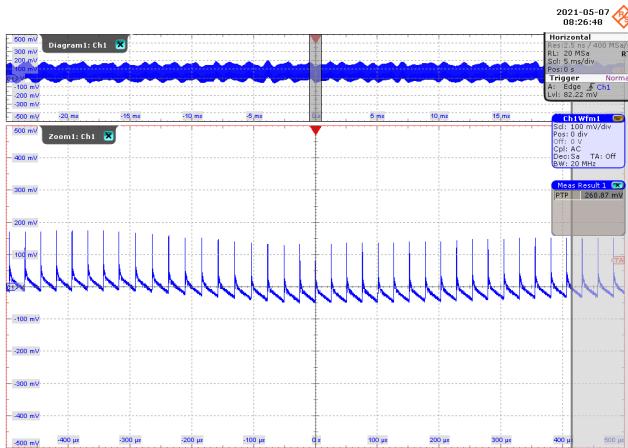


Figure 126 – 230 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
Zoom: 100 μ s / div.
Output Ripple = 260.87 mV.

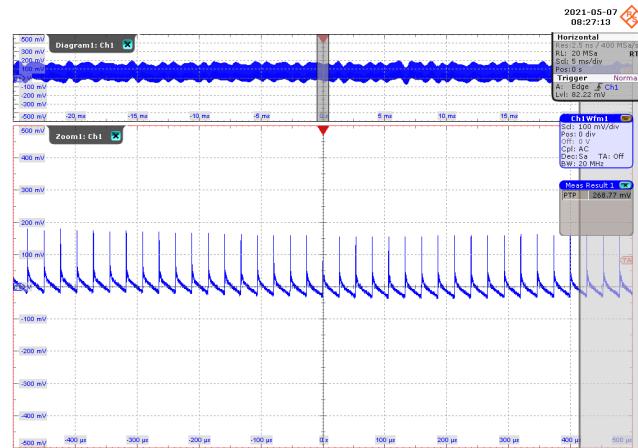


Figure 127 – 300 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
Zoom: 100 μ s / div.
Output Ripple = 268.77 mV.



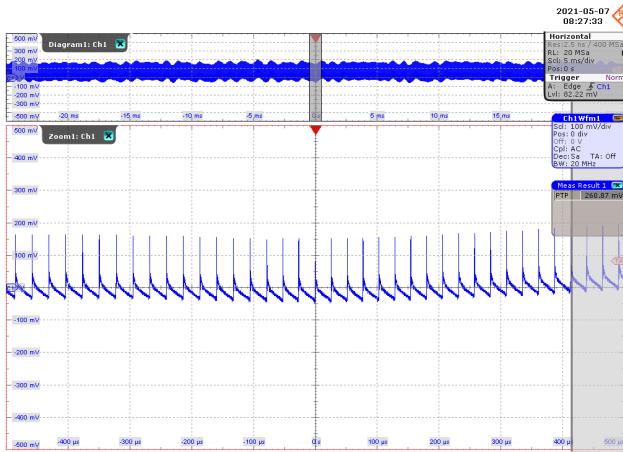


Figure 128 – 350 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 260.87 mV.

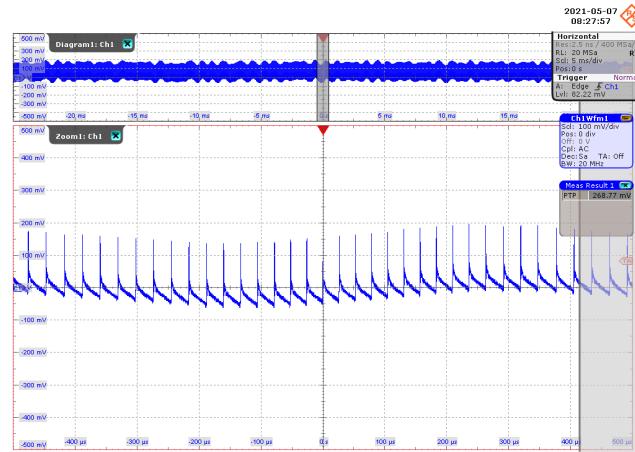


Figure 129 – 440 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 268.77 mV.

11.6.2.4 25% Load Condition

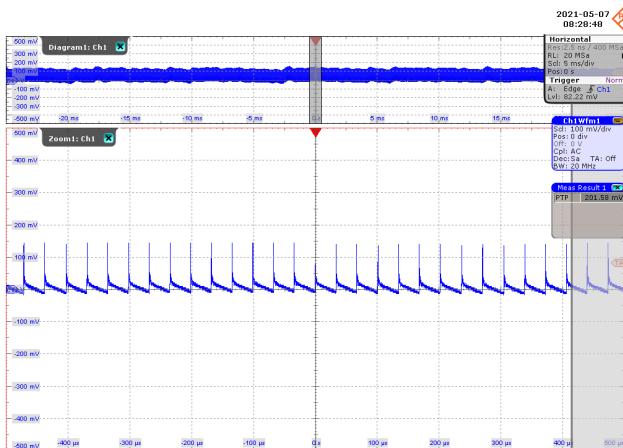


Figure 130 – 90 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 201.58 mV.

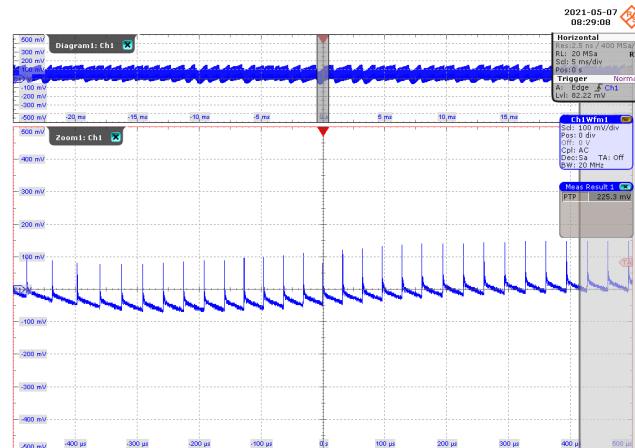


Figure 131 – 115 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 225.30 mV.



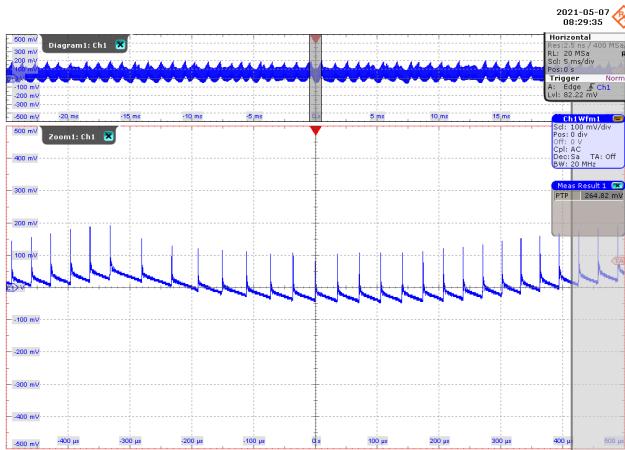


Figure 132 – 230 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 264.82 mV.

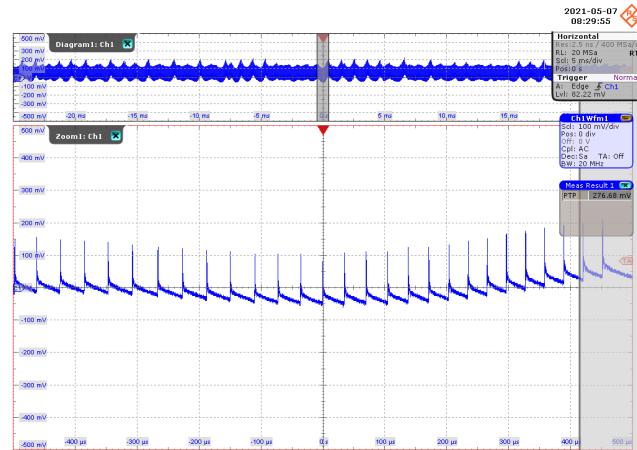


Figure 133 – 300 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 276.68 mV.

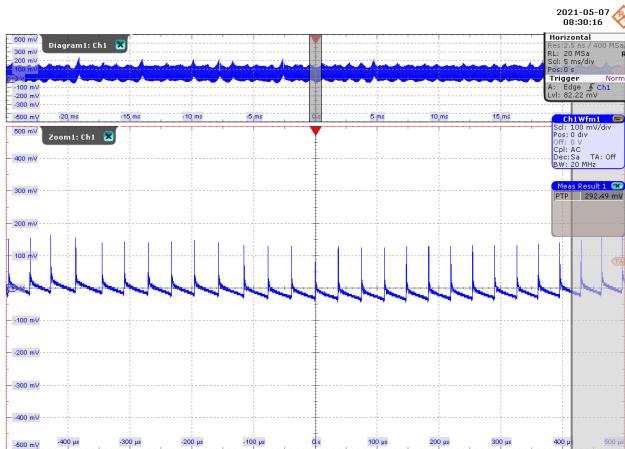


Figure 134 – 350 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 292.49 mV.

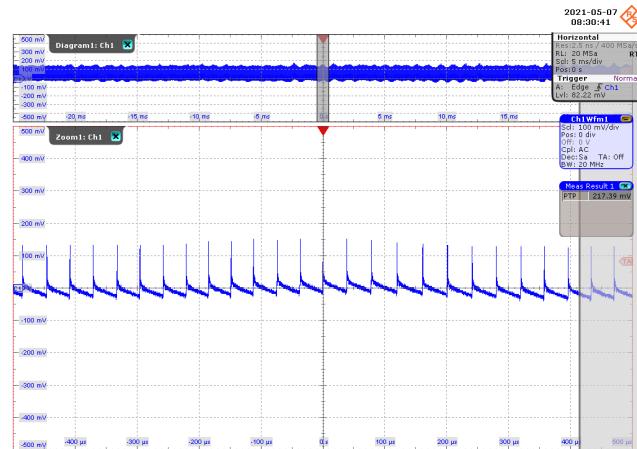


Figure 135 – 440 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 217.39 mV.



11.6.2.5 0% Load Condition

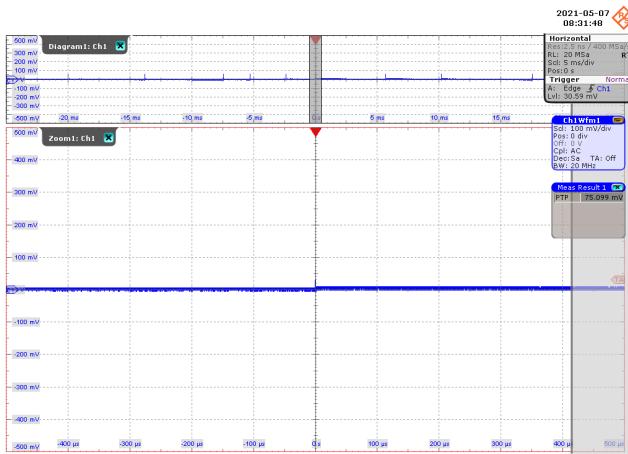


Figure 136 – 90 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
Zoom: 100 μ s / div.
Output Ripple = 75.10 mV.

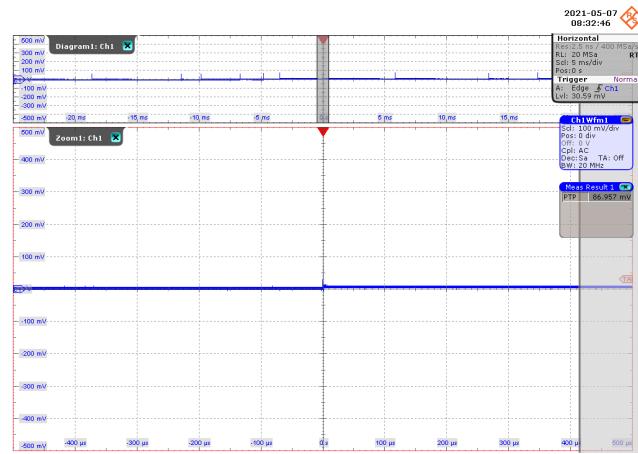


Figure 137 – 115 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
Zoom: 100 μ s / div.
Output Ripple = 86.96 mV.

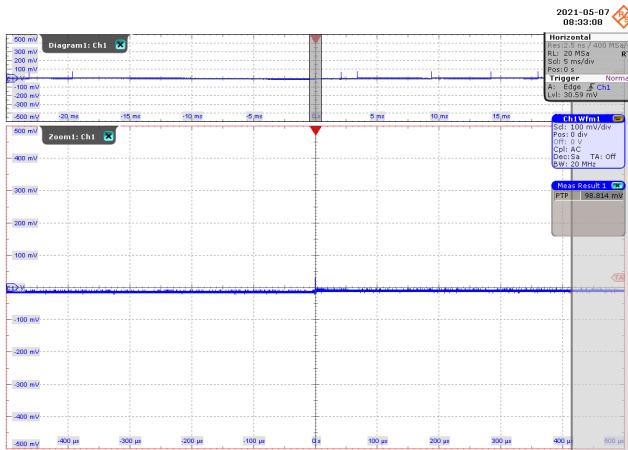


Figure 138 – 230 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
Zoom: 100 μ s / div.
Output Ripple = 98.81 mV.

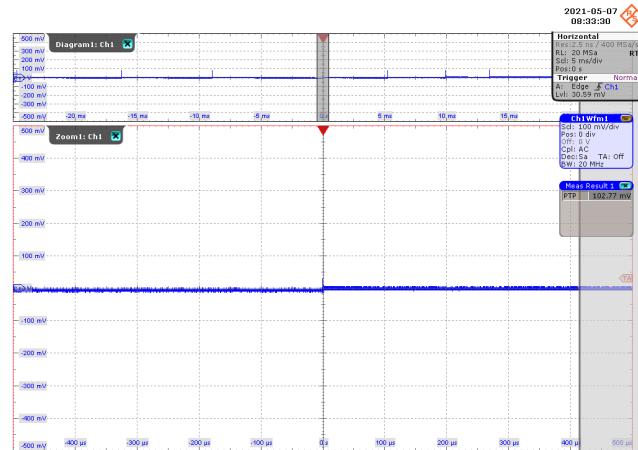


Figure 139 – 300 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
Zoom: 100 μ s / div.
Output Ripple = 102.77 mV.



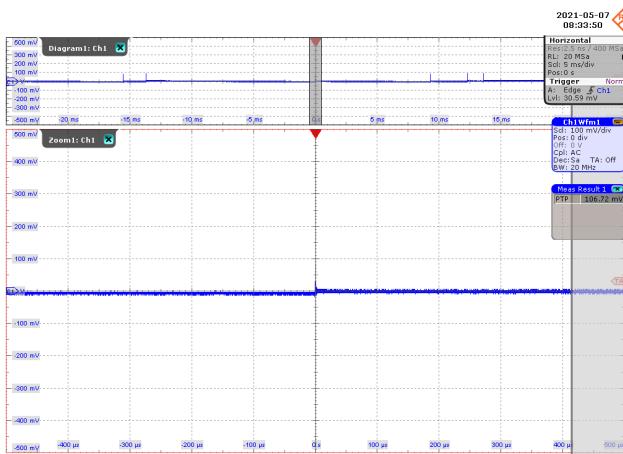


Figure 140 – 350 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 106.72 mV.

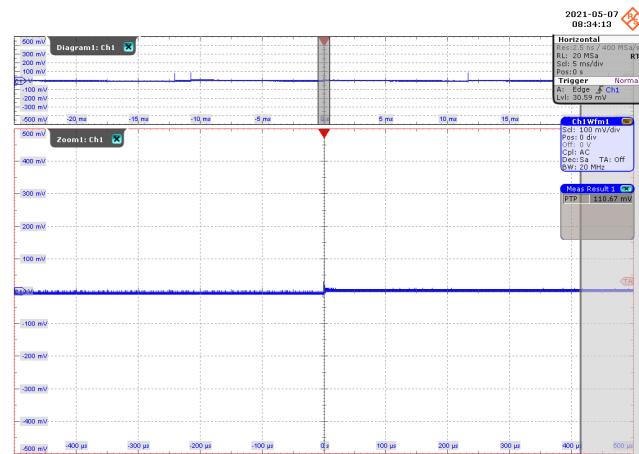


Figure 141 – 440 VAC 60 Hz.
CH1: V_{RIPPLE} , 100 mV / div., 5 ms / div.
 Zoom: 100 μ s / div.
 Output Ripple = 110.67 mV.



11.6.3 Output Ripple Voltage Graph from 0% - 100%

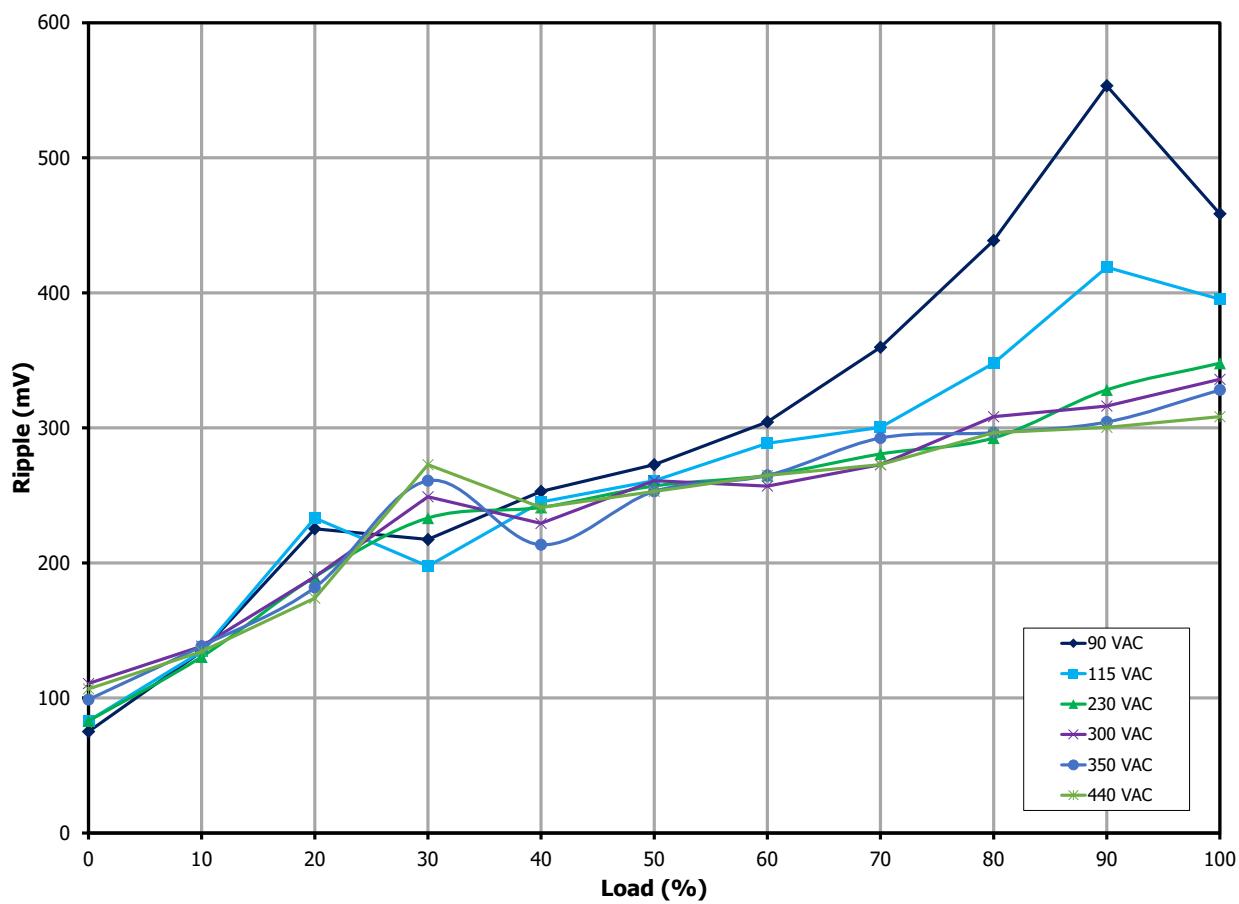


Figure 142 – Measured at the End of PCB, at Room Temperature.

12 Thermal Performance

12.1 Test Set-Up

Thermal evaluation was performed under two conditions: (1) room temperature and (2), ambient inside a thermal chamber. In both conditions, the circuit is soaked for at least an hour under full load conditions.



Figure 143 – Thermal Performance Set-up Using Thermal Chamber.

Thermal performance at 440 VAC 40 °C was also assessed using a heat spreader on the bottom side for better performance.

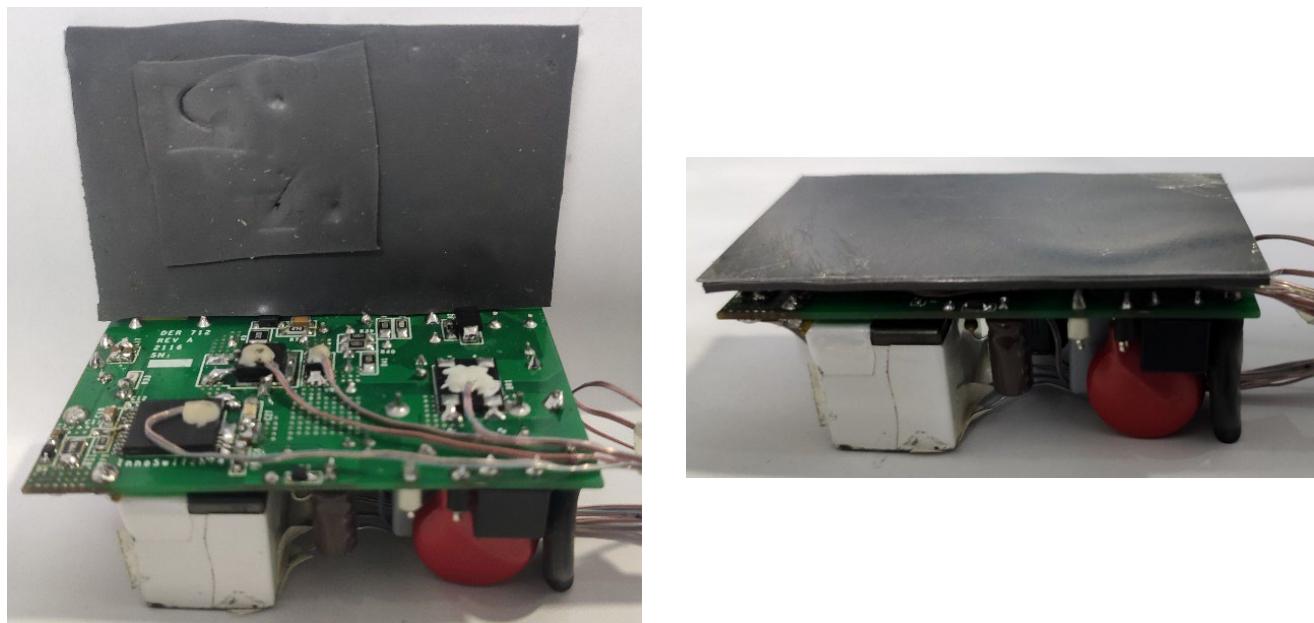


Figure 144 – 440 VAC 40 °C Set-up with Heat Spreader.



12.2 Thermal Performance at Room Temperature

12.2.1 90 VAC at Room Temperature

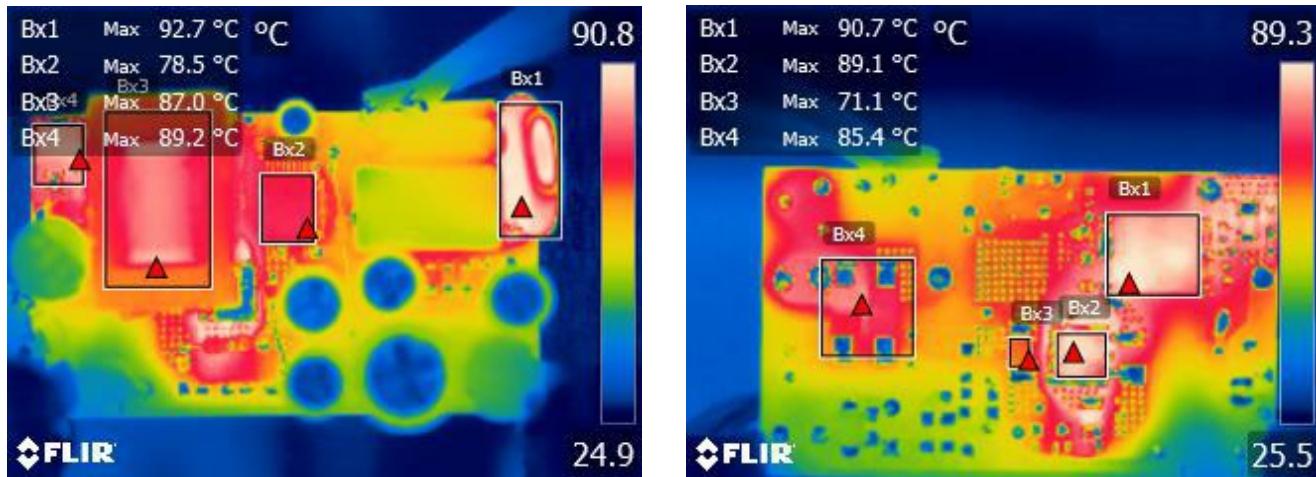


Figure 145 – Thermal Performance at 90 VAC.

Component	Temperature (°C)
Ambient	24.9
Thermistor (RT1)	92.7
MinE-CAP (U4)	78.5
Transformer (T2)	87.0
SR FET (Q2)	89.2
INN3679C (U1)	90.7
StackFET (Q3)	89.1
StackFET Clamp (VR2)	71.1
Bridge (BR1)	85.4



12.2.2 265 VAC at Room Temperature

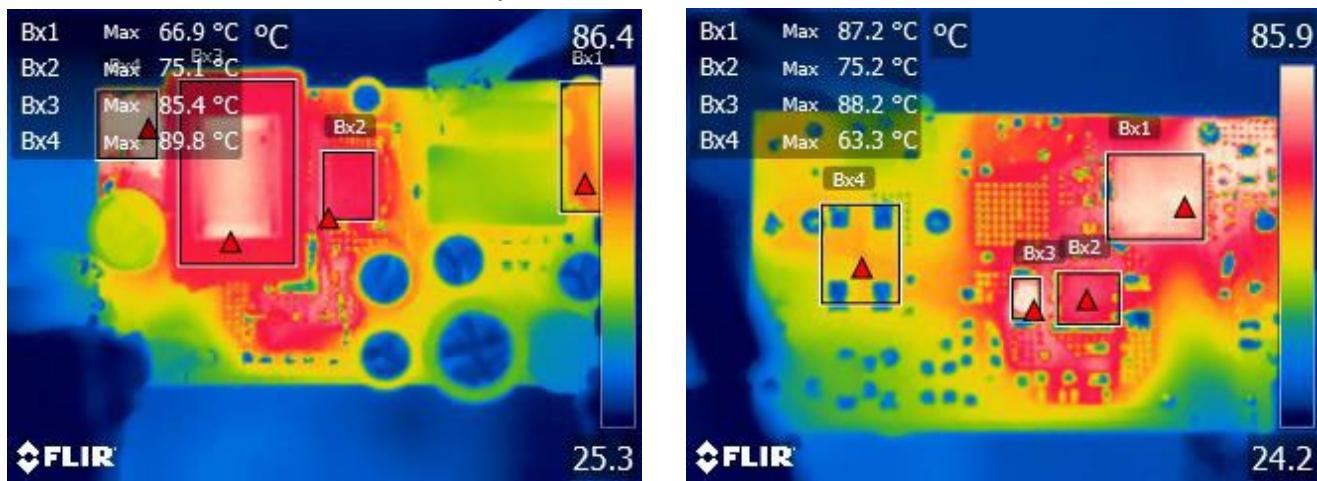


Figure 146 – Thermal Performance at 265 VAC.

Component	Temperature (°C)
Ambient	24.2
Thermistor (RT1)	66.9
MinE-CAP (U4)	75.1
Transformer (T2)	85.4
SR FET (Q2)	89.8
INN3679C (U1)	87.2
StackFET (Q3)	75.2
StackFET Clamp (VR2)	88.2
Bridge (BR1)	63.3



12.2.3 440 VAC at Room Temperature

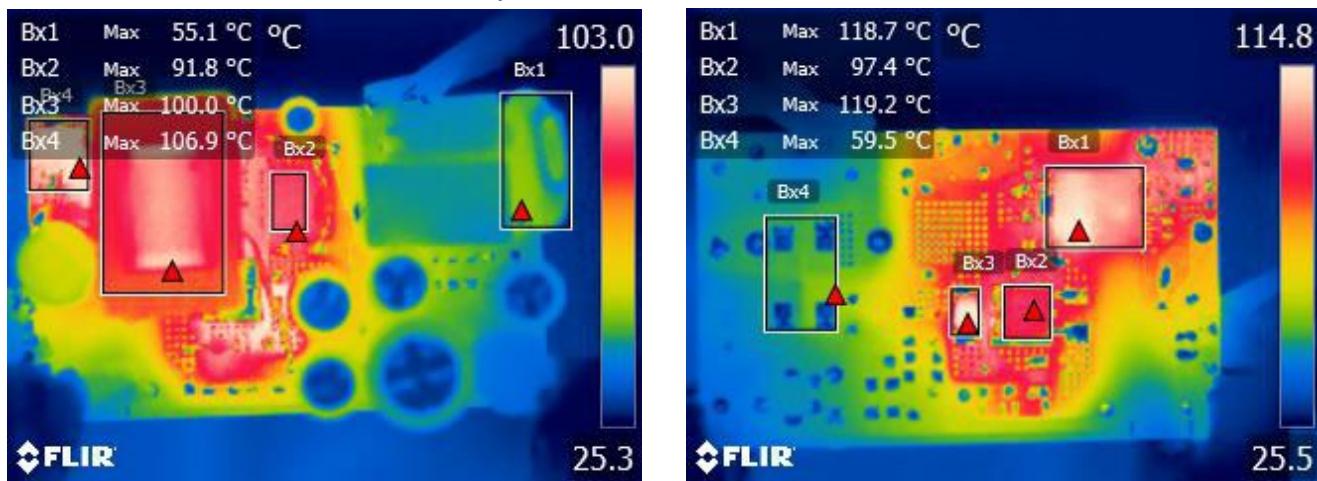


Figure 147 – Thermal Performance at 440 VAC.

Component	Temperature (°C)
Ambient	25.3
Thermistor (RT1)	55.1
MinE-CAP (U4)	91.8
Transformer (T2)	100.0
SR FET (Q2)	106.9
INN3679C (U1)	118.7
StackFET (Q3)	97.4
StackFET Clamp (VR2)	119.2
Bridge (BR1)	59.5



12.3 Thermal Performance at 40 °C

12.3.1 90 VAC at 40 °C

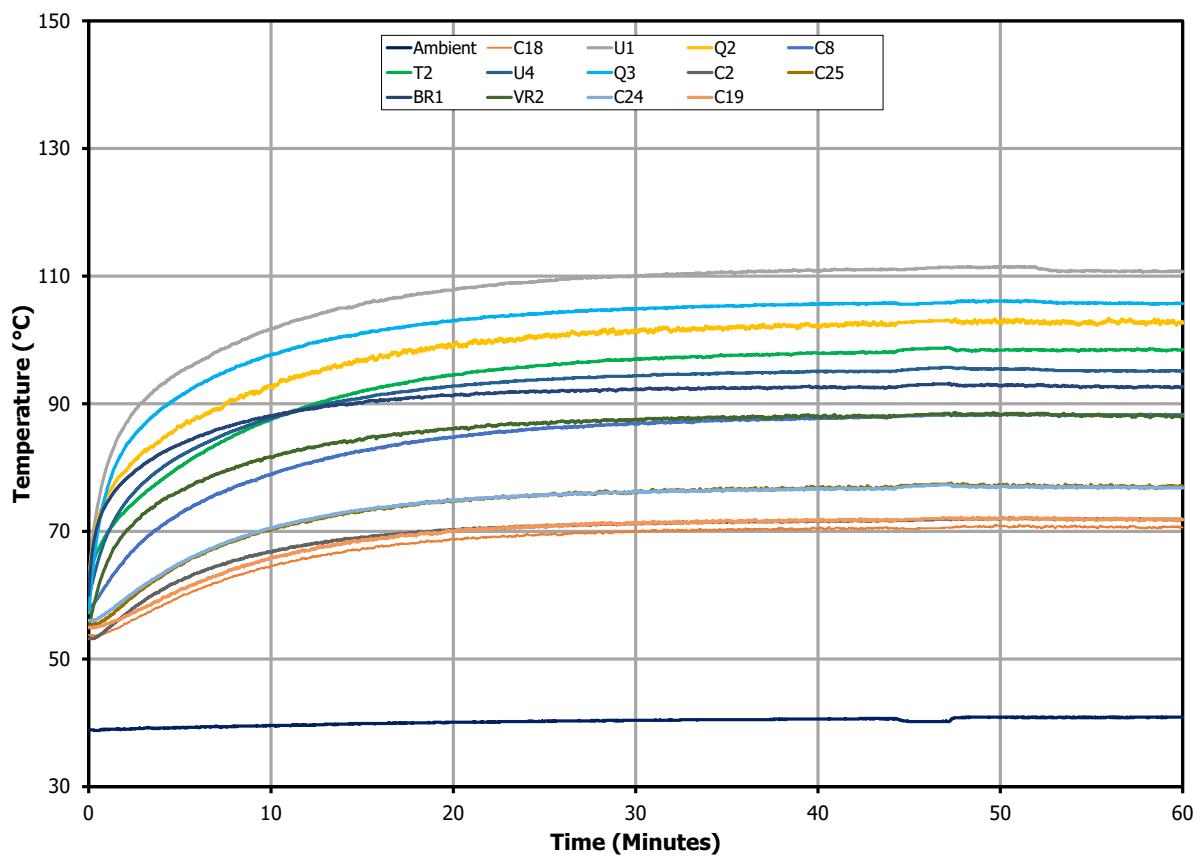
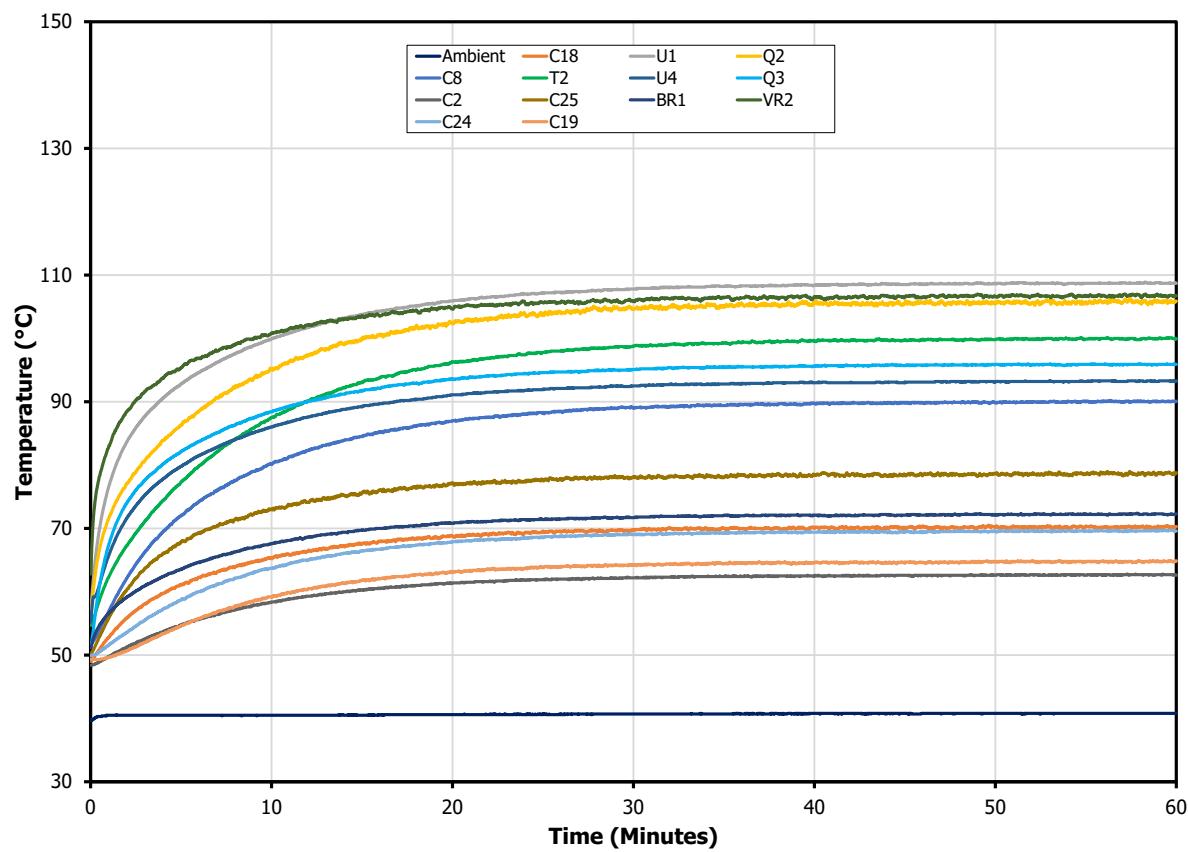


Figure 148 – Thermal Performance at 90 VAC, Full Load.

Component	Temperature (°C)
Ambient	40.9
HV_CAP1 (C18)	70.6
INN3679C (U1)	110.7
SR_FET (Q2)	102.6
Output Cap (C8)	88.3
Transformer (T2)	98.5
MinE-CAP (U4)	95.1
StackFET (Q3)	105.7
HV_CAP2 (C2)	71.9
HV_CAP3 (C25)	77.0
Bridge (BR1)	92.7
StackFET Clamp (VR2)	88.0
HV_CAP4 (C24)	76.8
LV_CAP (C19)	71.8

12.3.2 265 VAC at 40 °C

**Figure 149 – Thermal Performance at 265 VAC, Full Load.**

Component	Temperature (°C)
Ambient	40.8
HV_CAP1 (C18)	70.3
INN3679C (U1)	108.7
SR_FET (Q2)	105.9
Output Cap (C8)	90.1
Transformer (T2)	99.9
MinE-CAP (U4)	93.3
StackFET (Q3)	95.9
HV_CAP2 (C2)	62.6
HV_CAP3 (C25)	78.8
Bridge (BR1)	72.3
StackFET Clamp (VR2)	106.7
HV_CAP4 (C24)	69.6
LV_CAP (C19)	64.9

12.3.3 440 VAC at 40 °C

Time to reach OTP: 22 minutes

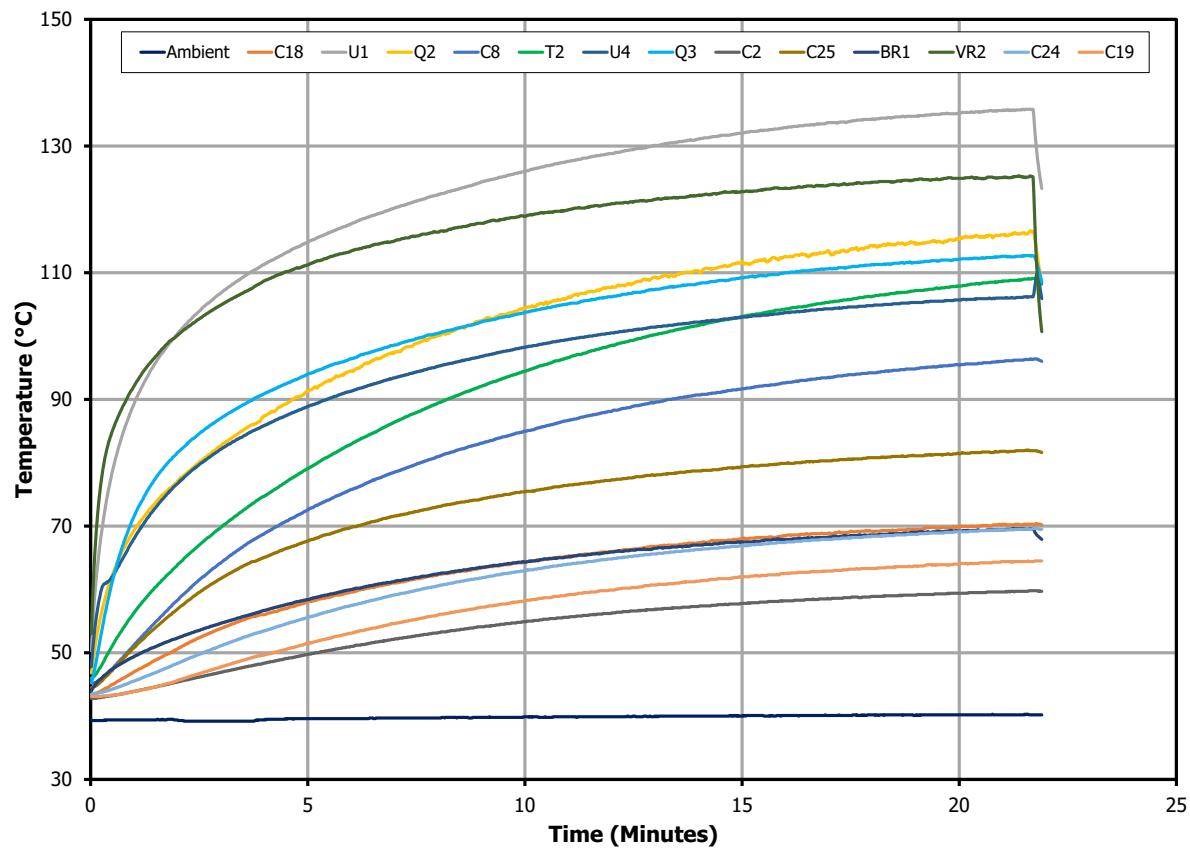


Figure 150 – Thermal Performance at 440 VAC, Full Load.

Component	Temperature (°C)
Ambient	40.2
HV_CAP1 (C18)	70.2
INN3679C (U1)	135.8
SR_FET (Q2)	116.5
Output Cap (C8)	96.3
Transformer (T2)	109.1
MinE-CAP (U4)	106.2
StackFET (Q3)	112.7
HV_CAP2 (C2)	59.8
HV_CAP3 (C25)	81.9
Bridge (BR1)	69.6
StackFET Clamp (VR2)	125.1
HV_CAP4 (C24)	69.6
LV_CAP (C19)	64.4

12.3.4 440 VAC at 40 °C, with Heat Spreader

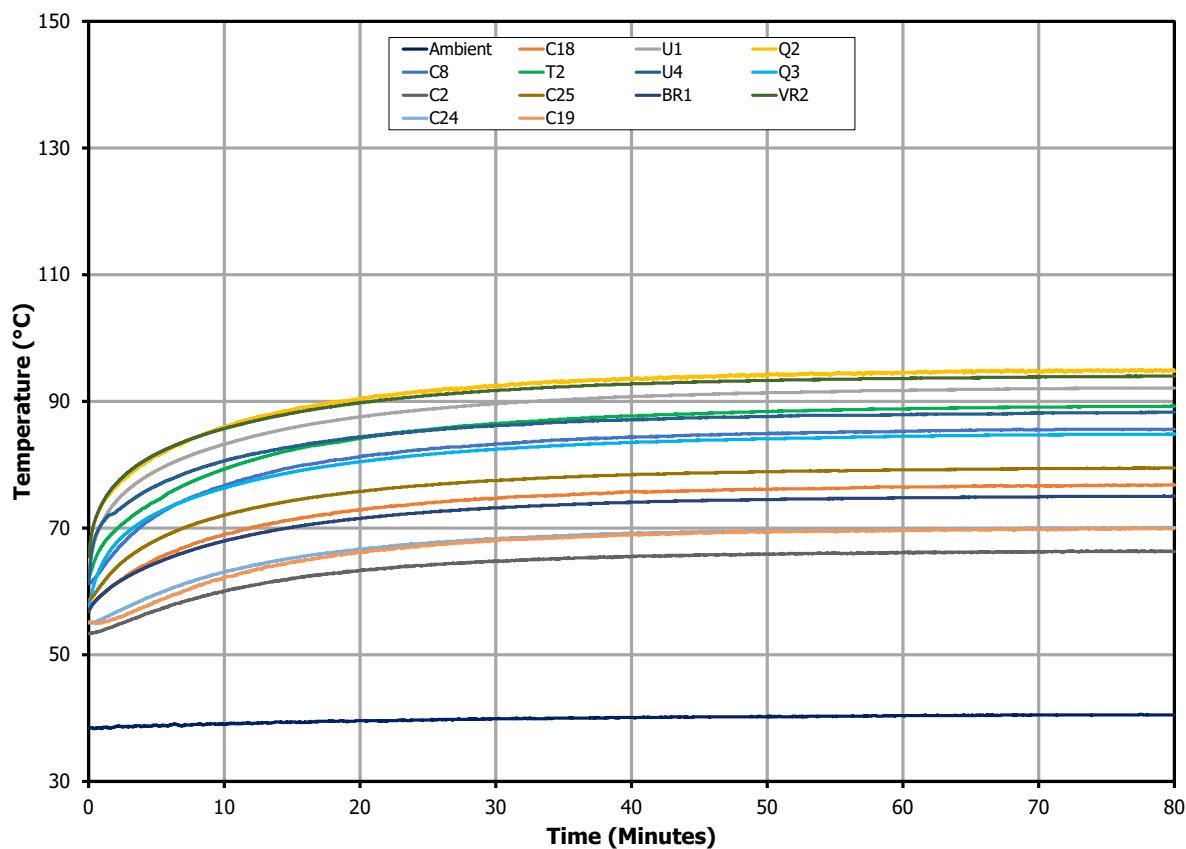


Figure 151 – Thermal Performance at 440 VAC with Heat Spreader, Full Load.

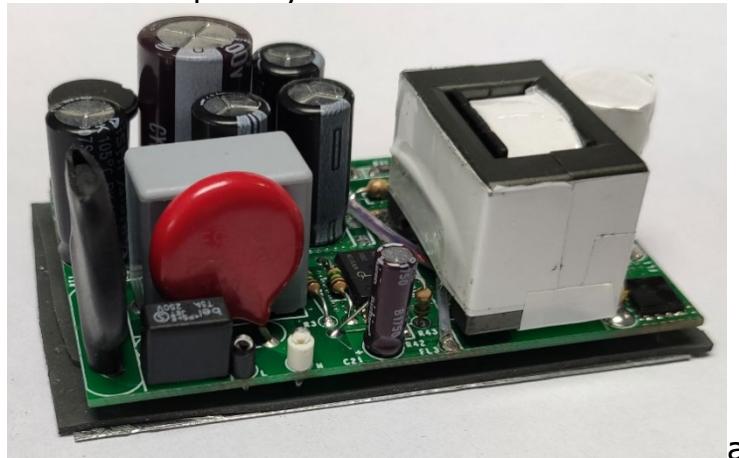
Component	Temperature (°C)
Ambient	40.5
HV_CAP1 (C18)	76.8
INN3679C (U1)	92.1
SR_FET (Q2)	94.7
Output Cap (C8)	85.6
Transformer (T2)	89.3
MinE-CAP (U4)	88.3
StackFET (Q3)	84.9
HV_CAP2 (C2)	66.3
HV_CAP3 (C25)	79.5
Bridge (BR1)	75.1
StackFET Clamp (VR2)	94.0
HV_CAP4 (C24)	70.1
LV_CAP (C19)	70.0

13 Conducted EMI

Conducted emissions tests were performed at 115 VAC and 230 VAC at full load (24 V, 2.5 A). Measurements were taken with output grounded and a 2m cable between the PCB and the resistor load.

13.1 Unit Set-up

Heat spreader on the bottom side is also implemented in the PSU for EMI shielding. Heat spreader is terminated to primary side GND.



13.2 Test Set-up Equipment

13.2.1 Equipment and Load Used

1. Rohde and Schwarz ENV216 two-line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Yokogawa WT310E power analyzer.
4. Chroma measurement test fixture.
5. Input voltage set at 115 VAC and 230 VAC.

13.3 Test Set-up

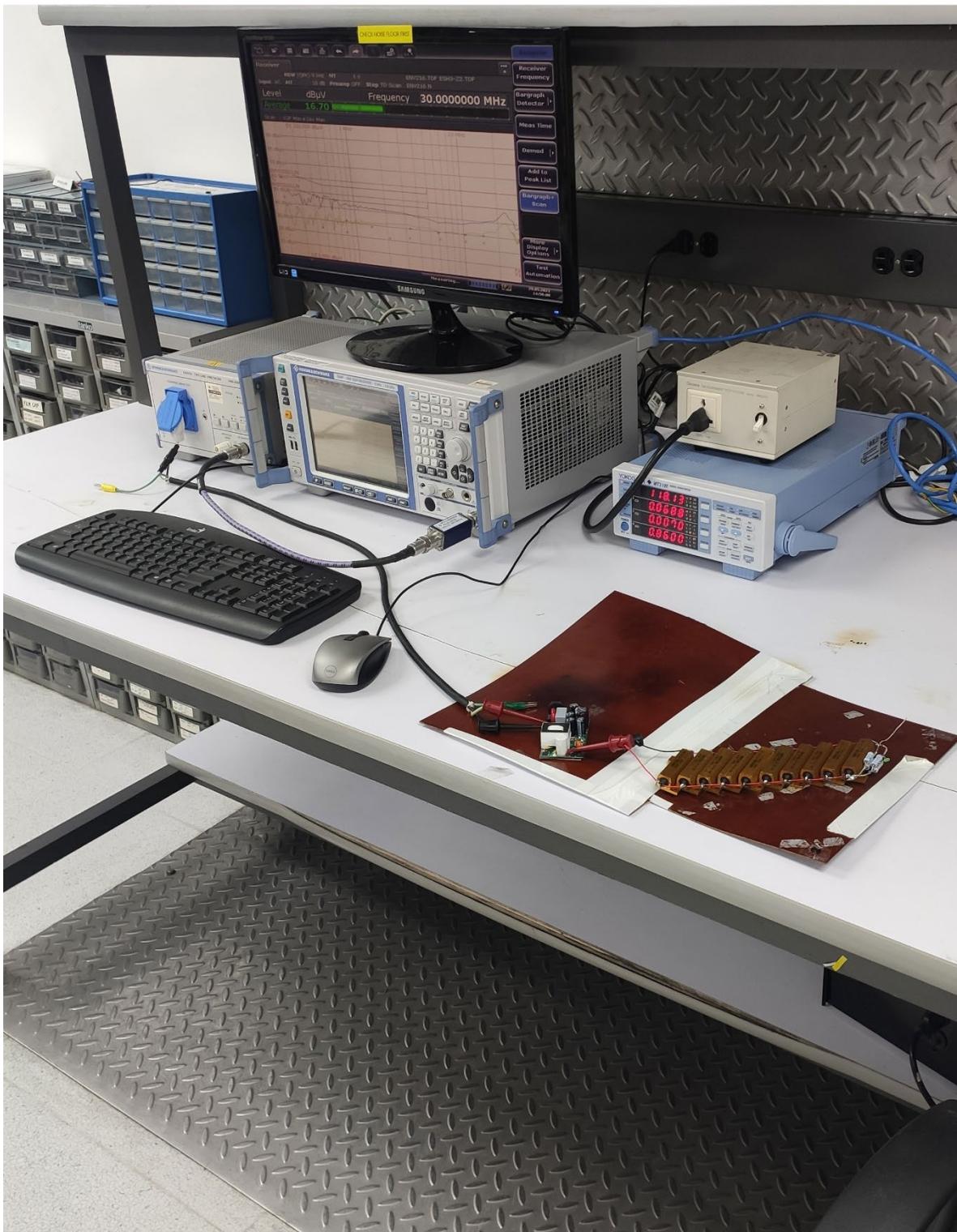
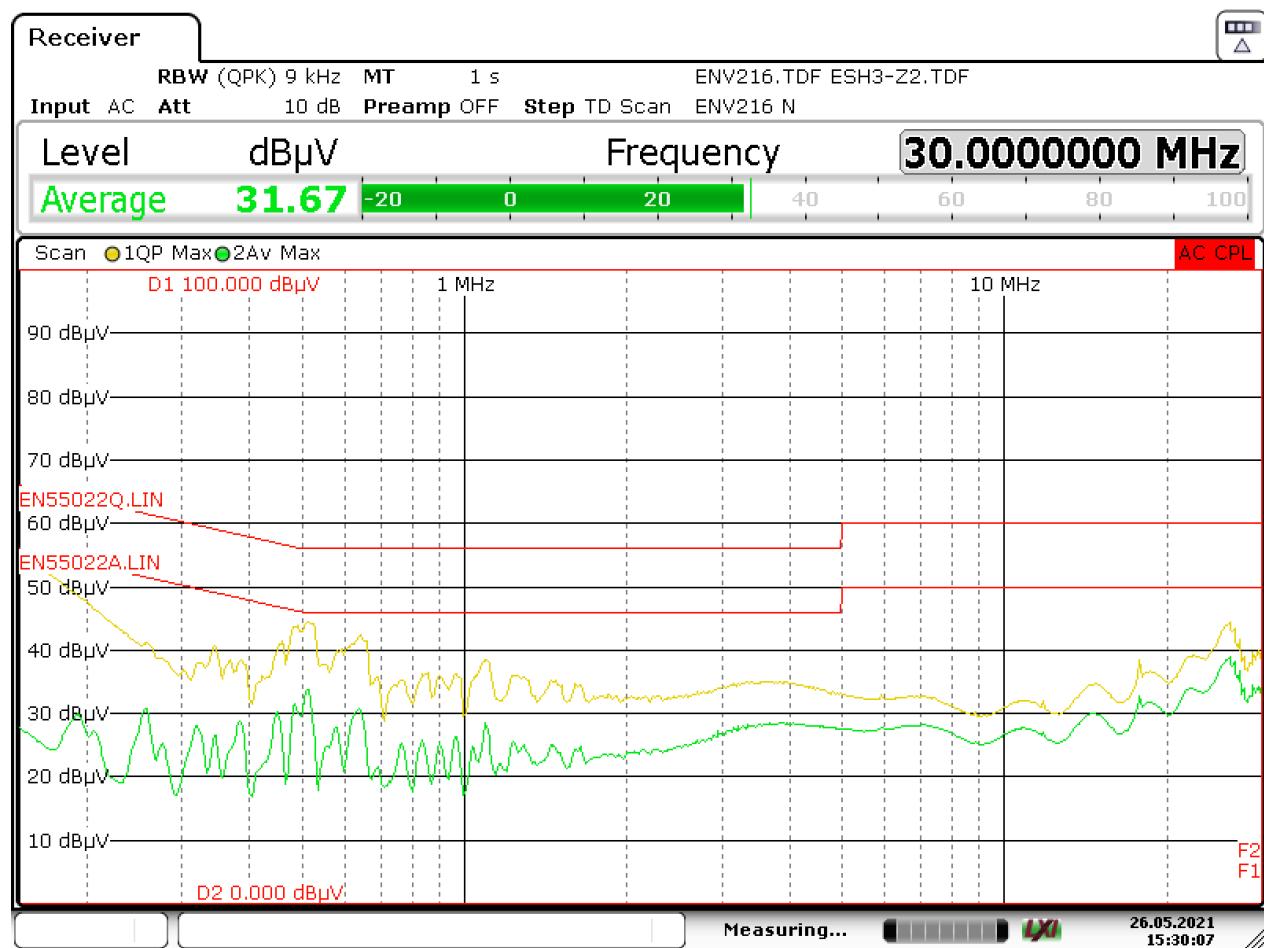


Figure 152 – EMI Test Set-up.



13.4 115 VAC 2.5 A Resistive Load

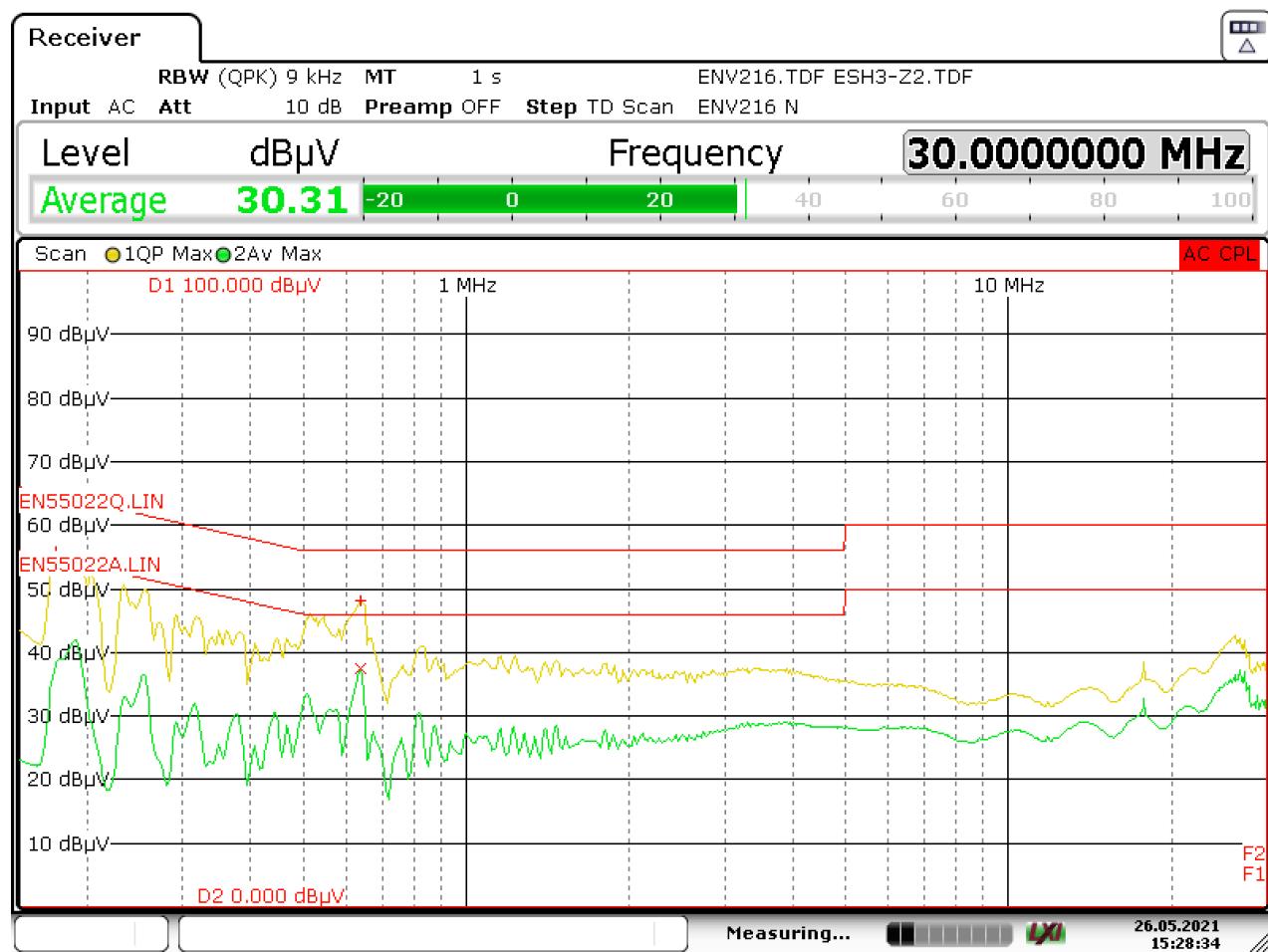


Date: 26.MAY.2021 15:30:08

Figure 153 – Floating Ground EMI at 115 VAC.



13.5 230 VAC 2.5 A Resistive Load



Date: 26.MAY.2021 15:28:34

Figure 154 – Floating Ground EMI at 230 VAC.



14 Line Surge

Differential input line surge testing was completed on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC / 60 Hz. Output was loaded at full load and operation was verified following each surge event.

14.1 Differential Mode Surge

DM Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
+5000	230	L to N	0	Pass, Class A
-5000	230	L to N	0	Pass, Class A
+5000	230	L to N	90	Pass, Class A
-5000	230	L to N	90	Pass, Class A
+5000	230	L to N	180	Pass, Class A
-5000	230	L to N	180	Pass, Class A
+5000	230	L to N	270	Pass, Class A
-5000	230	L to N	270	Pass, Class A



15 ESD

Note: ESD performance was tested on limited number of units. All ESD strikes were applied at end of cable.

Passed ±8 kV contact discharge

Contact Voltage (kV)	Applied to	Number of Strikes	Test Result
+8	VOUT	10	Pass
	GND	10	Pass
-8	VOUT	10	Pass
	GND	10	Pass

Note: In all PASS results, no damage observed.

Passed ±15 kV Air discharge

Air Discharge Voltage (kV)	Applied to	Number of Strikes	Test Result
+15	VOUT	10	Pass
	GND	10	Pass
-15	VOUT	10	Pass
	GND	10	Pass

Note: In all PASS results, no damage was observed.



16 Revision History

Date	Author	Revision	Description and Changes	Reviewed
15-Sep-21	VRA	1.0	Initial Release.	Apps & Mktg
10-Nov-21	KM	1.1	Fixed Figure 3	Apps & Mktg
28-Apr-22	RPA	1.2	Updated Surge Information, Transformer Specification and Assembly Instructions. Added Transformer Supplier.	Apps & Mktg
16-Aug-23	DK	1.3	Updated Schematic Figure 3.	Apps & Mktg



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